# Intermittently running AC motor 

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#### Abstract

In today's developed industry and commerce, the time and sequence required for each production process must be precisely controlled for manufactures of industrial products, otherwise all productions will fail. There are some examples for this rule. Biochemical pharmaceutical factories need precisely to control the operation time of the robot arm motor required for each procedure so that the grasping amount of each medicine is just right, so that the medicine can exert the best effect. Automatic factories use robotic arms to assemble car parts. The engineer adjusts the intermittent frequency of the intermittent operation motor according to the assembly time that is required for different parts to ensure smooth assembly and quality maintenance. Engineers adjust the frequency of intermittently running motors in the sequence control of the chemical plant to meet these needs of the production process. Engineers adjust the frequency of intermittently running motors according to these needs of different forging procedures in the operation of the chain steel plant. This approach allows each forging operation to completely improve the quality of the finished steel product, so that it can be sold at a good price in the market. There are so many applications for intermittently running motor.


Keywords-robot arms, sequence control, forging procedures, chain steel plant

## I. Introduction:

The paper can be divided into four parts. The first part is the generation of digital pulse. This part is composed of a function generator and a 555 astable multistage oscillator (only one of these two is used in actual operation). If the required frequency of the pulse wave is $f=1 \mathrm{~Hz}$, then we can use the 555 oscillator. If the required frequency of the pulse wave is not equal to 1 Hz , then we use a function generator instead. The second part is the modulus 16 synchronous counter and its display device. The third part is the intermittent operation control system (The system is paralleled from the modulus 16 synchronous counter). The fourth part is the AC motor system (The system is composed of operational amplifiers, relays, diodes, npn type BJT transistors and AC motors).

## II. Literature review:

For related research on "Intermittently running AC motors", here are some papers as examples. In literature [1], professor Dai Zhengfang researched and designed "Design of stepping motor high speed operation control circuit". The advantage of this design is to apply the design for the motor that needs the special application in industry. The disadvantage of this design is that if the industrial application level changes, then it must be redesigned. In literature [2], Mr. Li Hongkun researched and designed "AC motor starter and control device". The advantage of this design is that all analog electronic components are used for the simple structure and the low cost. The disadvantage of this design is that it cannot precisely control and adjust
the starting time of the motor. In literature [3], professor Zhuang Yongyan researched and designed "Combined characteristics of AC motor and frequency inverter". The speed of the AC motor depends entirely on the frequency. The advantage of this paper is that it can be applied to special medical engineering. The disadvantage of this paper is that the AC motor must be equipped with a feedback system to meet the stability requirements. In literature [4], Mr. Xu Maolin researched "AC motor (asynchronous motor)". The advantage of this paper is that the speed of the motor can be changed according to engineering needs of different stages. The disadvantage of this paper is that there will be a time delay in the conversion between different speeds. This disadvantage of this paper is not small. In literature [5], Mr. Xu Maolin researched "AC motor-synchronous motor". The advantage of this paper is that the motor can change the speed and rotation direction according to different stages of engineering application. When the motor speed changes, then the time delay is minimal and can be ignored.

## III. Explanation of principle:

(1) The electronic components used in this paper are as follows: $\oplus$ AC motor ( $110 \mathrm{~V}, 1 / 4 \mathrm{hp}$ ) \& logic IC 74LS191*1, 74LS32*1, 74LS83*1, 74LS11*1, 74LS47*1, 74LS20*1, 74LS76*1 ョanalog IC 555*1, © operation amplifier $\mu \mathrm{A} 741^{*} 15 \mathrm{npn}$ type BJT transistor 0 common anode 7-segment display $\varnothing$ LED light *5 8 resistance (1/4W): 200 ${ }^{*} 15$, $6.7 \mathrm{~K} \Omega^{*} 2,500 \Omega^{*} 2,5 \mathrm{~K} \Omega^{*} 1,15 \mathrm{~K} \Omega^{*} 1,1 \mathrm{~K} \Omega^{* 1} 9$ capacitance ( 50 W ): $0.01 \mu \mathrm{~F}^{\star} 1,100 \mu \mathrm{~F}^{\star} 1$ odiode ( number: IN4001)*1, ๑ relay (number:

TRD-12VDC-SB -CL) (12volt)* ${ }^{*}$.
(2) The wiring diagram of this paper is shown in Fig.1~Fig.4. Figure 1 is a schematic diagram of the overall architecture of this paper. Figure 2 is a detailed wiring diagram of the modulus 16 synchronous counter. Figure 3 is the operation diagram of the 555 oscillator. Figure 4 is a detailed wiring diagram of the intermittent operation control system.
(3) "SW1" in figure 1 represents the switch between the function generator and the 555 astable multistage oscillator. If the frequency of the digital pulse is $\mathrm{f}=1 \mathrm{~Hz}$, then the best choice is the 555 oscillator. The stability of the pulse wave of the 555 oscillator is better. At this time, the running time and stopping time of the AC motor are both 8 seconds. In the other words, the sum of each running and stopping time is 16 seconds (This is definition of modulus 16). If the intermittent operation time of the AC motor is not 8 seconds in actual application, then the "SW1" switch will be transfer to the function generator. At the same time, the frequency value can be adjusted according to actual needs. The conversion principle of this part will be explained later.
(4) The digital output $Q_{3} Q_{2} Q_{1} Q_{0(2)}$ is connected in parallel to 2 -bit common anode 7 - segment LED display and intermittent operation control system as shown in figure 1. In this way, it can precisely check whether the intermittent movement starts on time and closes on time or not.


## Fig. 1 The schematic diagram of the overall system configuration



Fig. 2 The detailed wiring diagram of mode 16 synchronous counter


Fig.3a The current path for the first charging


Fig.3b The current path for the discharging


Fig.3c The current path for the second charging


Fig.3d The output pulse of the 555 oscillator

Fig. 3 The operation of the 555 oscillator


Fig. 4 The detailed wiring diagram of the control system for intermittently running

## IV. The principle of 555

## astable multistage oscillator

(1) In figure $3 a$, the broken line represents the trajectory of the current through the 555 oscillator during the first charging process. The current starts from point e and goes through points $a, ~ b, ~ c, ~ d$ and finally flows to point $g$ (grounding) $(e \rightarrow a \rightarrow b \rightarrow c \rightarrow$ $d \rightarrow g$ ). There are two paths for current to choose at point a. Because the internal resistance of the diode $R_{D}=5 \Omega$ is much smaller than $R_{F}=7.2 \mathrm{~K} \Omega$, therefore the current must flow through the low resistance route $(\mathrm{e} \rightarrow \mathrm{a} \rightarrow \mathrm{b} \rightarrow \mathrm{c} \rightarrow \mathrm{d} \rightarrow \mathrm{g})$ and not flow through the high resistance route $(\mathrm{e} \rightarrow \mathrm{a} \rightarrow \mathrm{d} \rightarrow$ g). At this time, the output voltage $\left(\mathrm{V}_{3}=\mathrm{V}_{\text {out }}\right)$ of the 555 oscillator is DC bia voltage $\mathrm{V}_{\mathrm{CC}}\left(\mathrm{V}_{\text {out }}=\mathrm{V}_{3}=\mathrm{V}_{\mathrm{CC}}=\right.$ 5 V ) (high potential /). Because figure 3 a is the first charging, therefore its charging time $t_{0}$ is transient.
(2) In figure 3 b , the broken line represents the trajectory of the current through all discharging processes. The current starts from point g . The cb route is closed due to the backstop effect of the diode at point g , so the current has only one choice. The current passes through the $R_{F}$ resistance and then enters the 555 oscillator from pin $7(g \rightarrow d \rightarrow$ $a \rightarrow 7$ ) (here " 7 " refers to the 7th pin of 555 oscillator). At this time, the output voltage $\mathrm{V}_{3}\left(\mathrm{~V}_{\text {out }}\right)$ of the 555 oscillator is low potential " $\phi$ ". The time required for all discharging processes is all the same as $t_{1}$ (second).
(3) According to the discharging route $(\mathrm{g} \rightarrow \mathrm{d} \rightarrow \mathrm{a} \rightarrow 7$ ) in figure $3 b$. The time $t_{1}$ required for the discharging is calculated as following.

$$
\begin{aligned}
t_{1}= & R_{F}{ }^{*} C^{*}(\ln 2)=\left(7.2 \times 10^{3}\right) X\left(100 \times 10^{-6}\right) X(\ln 2)=0.5( \\
& \text { sec })
\end{aligned}
$$

(4) In figure 3c, the current follows the charging path after the second charging $(\mathrm{e} \rightarrow \mathrm{a} \rightarrow \mathrm{b} \rightarrow \mathrm{c} \rightarrow \mathrm{d} \rightarrow \mathrm{g})$ to calculate the charging time $t_{2}$ after the second charging (considering the internal resistance of the diode $R_{D}=5 \Omega$ ).
$\mathrm{t}_{2}=\left(\mathrm{R}_{\mathrm{E}}+\mathrm{R}_{\mathrm{D}}\right)^{*} \mathrm{C}^{*} \ln 2=\left(7.2 \times 10^{-6}+5\right) \Omega \mathrm{X}\left(100 \times 10^{-6} \mathrm{~F}\right) \mathrm{X}(\mathrm{ln}$
2)=0.5(sec)
(5) The output pulse wave excluding the first charging is shown in figure 3d. The period $T$ and frequency $f$ are calculated as followings.

$$
\begin{aligned}
& \mathrm{T}=\mathrm{t}_{1}+\mathrm{t}_{2}=0.5+0.5=1(\mathrm{sec}) \\
& \mathrm{f}=1 / \mathrm{T}=1 /(1 \mathrm{sec})=1(\mathrm{~Hz})
\end{aligned}
$$

(6) Connect the output pulse wave (digital pulse wave) of figure $2 d$ to the 14th pin of IC74191 in figure 1.
V. The digital logic conversion of the intermittent operation control system:
(1) When the output of the logic IC74191 is $\mathrm{Q}_{3} \mathrm{Q}_{2} \mathrm{Q}_{1} \mathrm{Q}_{0}=\phi \phi \phi \phi_{(2)}=0_{(10)}$, then the output of J-K flip-flop is shown in figure 6a. For the J-K flip-flop, when_PR and $\underline{C L}$ are / (high potential) simultaneously, then the output will maintain the previous state. Because the front output of the J-K flip-flop is $\phi$ (low potential), therefore the output of this trigger is still the same as $\phi$ (low potential).
(2) When the output of the logic IC74191 is $\mathrm{Q}_{3} \mathrm{Q}_{2} \mathrm{Q}_{1} \mathrm{Q}_{0}=\phi / / \phi_{(2)}=6_{(10)}$, then the output of J-K flip-flop is shown in figure 6b. For the J-K flip-flop, when the case of $\underline{\mathrm{PR}}=/$ and $\underline{\mathrm{CL}}=\phi$ occur, then the output of this trigger is $\phi$ (low potential).
(3) When the output of the logic IC74191 is $\mathrm{Q}_{3} \mathrm{Q}_{2} \mathrm{Q}_{1} \mathrm{Q}_{0}=\phi / / /(2)=7_{(10)}$, then the output of $\mathrm{J}-\mathrm{K}$ flip-flop is shown in figure 6c. For the J-K flip-flop, when the case of $\underline{\mathrm{PR}}=\phi$ and $\underline{C L=/ ~ o c c u r, ~ t h e n ~ t h e ~}$ output of this trigger is / (high potential).
(4) When the output of the logic IC74191 is $Q_{3} Q_{2} Q_{1} Q_{0}=/ \phi / \phi_{(2)}=10_{(10)}$, then the output of J-K flip-flop is shown in figure 6d. For the J-K flip-flop, when $\quad \mathrm{PR}$ and $\underline{C L}$ are / (high potential) simultaneously, then the output will maintain the previous state. Because the front output of the J-K flip-flop is / (high potential), therefore the output of this trigger is still the same as / (high potential).
(5) When the output of the logic IC74191 is
$Q_{3} Q_{2} Q_{1} Q_{0}=/ / \phi /_{(2)}=13_{(10)}$, then the output of J-K flip-flop is shown in figure 6e. For the J-K flip-flop, when_ PR and CL are / (high potential) simultaneously, then the output will maintain the previous state. Because the front output of the J-K flip-flop is / (high potential), therefore the output of this trigger is still the same as / (high potential).
(6) When the output of the logic IC74191 is $Q_{3} Q_{2} Q_{1} Q_{0}=/ / / \phi_{(2)}=14_{(10)}$, then the output of J-K flip-flop is shown in figure 6f. For the J-K flip-flop, when $\underline{\mathrm{PR}}=/$ and $\underline{\mathrm{CL}}=\phi$ occur, then the output of this trigger is $\phi$ (low potential).
(7) When the output of the logic IC74191 is
$\mathrm{Q}_{3} \mathrm{Q}_{2} \mathrm{Q}_{1} \mathrm{Q}_{0}=/ / / /(2)=15_{(10)}$, then the output of J-K flip-flop is shown in figure 6 g . For the J-K flip-flop, when_ PR and $\underline{\mathrm{CL}}$ are / (high potential) simultaneously, then the output will maintain the previous state. Because the front output of the J-K flip-flop is $\phi$ (low potential), therefore the output of this trigger is still the same as $\phi$ (low potential).
(8) Combining the descriptions of points (1) ~ (7) above can be shown in figure 5 . Figure 5 represents the relationship between the J-K flip-flop and the pulse wave.


# Fig.5 The realionship diagran befween the pulse wave and the ouptuto J J.-Kipiplop 





Fig.6a The output of J-K flip-flop in the case of $Q_{3} Q_{2} Q_{1} Q_{0}=\phi \phi \phi \phi_{(2)}=0_{(10)}$ (keep the original condition)


Fig.6c The output of J-K flip-flop in the case of $Q_{3} Q_{2} Q_{1} Q_{0}=\phi / /{ }_{(2)}=7_{(10)}$ (high potential)


Fig.6b The output of J -K flip-flop in the case of $\mathrm{Q}_{3} \mathrm{Q}_{2} \mathrm{Q}_{1} \mathrm{Q}_{0}=\phi / / \phi_{(2)}=6_{(10)}$
(keep the original condition)


Fig.6d The output of J-K flip-flop in the case of $\mathrm{Q}_{3} \mathrm{Q}_{2} \mathrm{Q}_{1} \mathrm{Q}_{0}=/ \phi / \phi_{(2)}=10_{(10)}$
(keep the original condition)


Fig.6e The output of J -K flip-flop in the case of $\mathrm{Q}_{3} \mathrm{Q}_{2} \mathrm{Q}_{1} \mathrm{Q}_{0}=/ / \phi /{ }_{(2)}=13_{(10)}$ (keep the original condition)

Fig. 6 g The output of $\mathrm{J}-\mathrm{K}$ flip-flop in the case of $\mathrm{Q}_{3} \mathrm{Q}_{2} \mathrm{Q}_{1} \mathrm{Q}_{0}=/ / / /{ }_{(2)}=15_{(10)}$ (keep the original condition)



Fig.6f The output of $\mathrm{J}-\mathrm{K}$ flip-flop in the case of $\mathrm{Q}_{3} \mathrm{Q}_{2} \mathrm{Q}_{1} \mathrm{Q}_{0}=/ / / \phi_{(2)}=14_{(10)}$
(low potential)

Fig. 6 The logic change diagrams of the intermittently operation system
VI. The logic circuit principle of a 2-bit common $\mathrm{B}_{3} \mathrm{~B}_{2} \mathrm{~B}_{1} \mathrm{~B}_{0}=\mathrm{S}_{3}{ }^{\prime} \mathrm{S}_{2}{ }^{\prime} \mathrm{S}_{1}{ }^{\prime} \mathrm{S}_{0} "\left(/ / / /{ }_{(2)}+\phi / / \phi_{(2)}=\phi / \phi /_{(2)}\right)$.
(1) When the output of logic IC74191 is $Q_{3} Q_{2}$ $Q_{1} Q_{0(2)}=\phi \phi / \phi_{(2)}=2_{(10)}$, how to display " 2 " on the 7-segment LED display in figure 7a with Arabic numerals that humans can understand. In figure 7a, the logic IC7483 is a 4-bit binary full adder. $\mathrm{S}_{3} \mathrm{~S}_{2} \mathrm{~S}_{1} \mathrm{~S}_{0}+\mathrm{B}_{3} \mathrm{~B}_{2} \mathrm{~B}_{1} \mathrm{~B}_{0}=\mathrm{S}_{3}{ }^{"} \mathrm{~S}_{2}{ }^{"} \mathrm{~S}_{1}{ }^{"} \mathrm{~S}_{0}{ }^{"}$
$\left(\phi \phi / \phi_{(2)}+\phi \phi \phi \phi_{(2)}=\phi \phi / \phi_{(2)}\right)$. IC7447(a) and the trailing 7-segment LED display are used to display the position of the ten's place. IC7447(b) and the trailing 7-segment LED display are used to display the position of the one's place.
(2) When the output of logic IC74191 is $Q_{3} Q_{2}$ $\mathrm{Q}_{1} \mathrm{Q}_{0(2)}=/ \phi \phi /{ }_{(2)}==_{(10)}$, how to display " 9 " on the 7-segment LED display in figure 7b with Arabic numerals that humans can understand. $\mathrm{S}_{3} \mathrm{~S}_{2} \mathrm{~S}_{1} \mathrm{~S}_{0}+$ $\mathrm{B}_{3} \mathrm{~B}_{2} \mathrm{~B}_{1} \mathrm{~B}_{0}=\mathrm{S}_{3} " \mathrm{~S}_{2}{ }^{\prime} \mathrm{S}_{1} " \mathrm{~S}_{0} "\left(/ \phi \phi /_{(2)}+\phi \phi \phi \phi_{(2)}=/ \phi \phi /_{(2)}\right)$
(3) When the output of logic IC74191 is $Q_{3} Q_{2}$ $Q_{1} Q_{0(2)}=/ / \phi \phi_{(2)}=12_{(10)}$, how to display " 12 " on the 7-segment LED display in figure 7c with Arabic numerals that humans can understand. $\mathrm{S}_{3} \mathrm{~S}_{2} \mathrm{~S}_{1} \mathrm{~S}_{0}+$ $\mathrm{B}_{3} \mathrm{~B}_{2} \mathrm{~B}_{1} \mathrm{~B}_{0}=\mathrm{S}_{3}{ }^{\prime} \mathrm{S}_{2}{ }^{\prime} \mathrm{S}_{1}{ }^{\prime} \mathrm{S}_{0}$ " $\left(/ / \phi \phi_{(2)}+\phi / / \phi_{(2)}=\phi \phi / \phi_{(2)}\right)$
(4) When the output of logic IC74191 is $Q_{3} Q_{2}$ $Q_{1} Q_{0(2)}=/ / / / /_{(2)}=15_{(10)}$, how to display " 15 " on the 7-segment LED display in figure 7d with Arabic numerals that humans can understand. $\mathrm{S}_{3} \mathrm{~S}_{2} \mathrm{~S}_{1} \mathrm{~S}_{0}+$


Fig.7a The logic diagram of the timing display in the case of $\mathrm{Q}_{3} \mathrm{Q}_{2} \mathrm{Q}_{1} \mathrm{Q}_{0}=\phi \phi / \phi_{(2)}=2_{(10)}$


Fig.7b The logic diagram of the timing display in the case of $\mathrm{Q}_{3} \mathrm{Q}_{2} \mathrm{Q}_{1} \mathrm{Q}_{0}=/ \phi \phi /(2)=9_{(10)}$


Fig.7c The logic diagram of the timing display in the case of $Q_{3} Q_{2} Q_{1} Q_{0}=/ / \phi \phi_{(2)}=12_{(10)}$


Fig.7d The logic diagram of the timing display in the case of $Q_{3} Q_{2} Q_{1} Q_{0}=/ / / / /_{(2)}=15_{(10)}$

Fig. 7 The logic diagram of the timing display


Fig. 8 When the output of IC 7476 is $\phi$ (low potential), then the AC motor stops


Fig. 9 When the output of IC 7476 is /
(high potential), then the AC motor runs

## VII. The principle of the AC motor

(1) Calculate the negative terminal voltage $\mathrm{V}_{-}\left(\mathrm{V}_{-}=\mathrm{V}_{2}\right)$ of the operational amplifier in figure 8 and figure 9 using the voltage division rule.
$\mathrm{V} .\left(\mathrm{V}_{2}\right)=13 \mathrm{~V} * \frac{1 \mathrm{~K} \Omega}{(15+1) \mathrm{K} \Omega}=0.8 \mathrm{~V}-\cdots---\Phi$
(2) Because the output of logic IC7476 in figure 8 is $\mathrm{Q}=\phi$ (low potential), therefore the positive terminal voltage of the operational amplifier is $\mathrm{V}_{+}\left(\mathrm{V}_{3}\right)=0$ (volt). Because $\left(\mathrm{V}_{+}=\mathrm{V}_{3}=0 \mathrm{v}\right)<\left(\mathrm{V}_{-}=\mathrm{V}_{2}=0.82 \mathrm{v}\right)$, then the output voltage $\mathrm{V}_{6}$ of the operational amplifier is negative $\left[\mathrm{V}_{6}\left(\mathrm{~V}_{\text {out }}\right)=-13 \mathrm{v}\right]$. At the same time, the BJT transistor is closed and the relay is also closed (that is, normally open). The AC current is interruption and the AC motor also stops.
(3) Because the output of the logic IC7476 in figure 9 is $\mathrm{Q}=/$ (high potential), therefore the positive terminal voltage of the operational amplifier is $\mathrm{V}_{+}=\mathrm{V}_{3}=2.1 \mathrm{v}$. Because of $\left(\mathrm{V}_{+}=\mathrm{V}_{3}=2.1 \mathrm{v}\right)>\left(\mathrm{V}_{-}=\mathrm{V}_{2}=0.82 \mathrm{v}\right)$, then the output voltage $\mathrm{V}_{6}$ is positive $\left[\mathrm{V}_{6}\left(\mathrm{~V}_{\text {out }}\right)=13 \mathrm{v}\right]$.
(4) Assuming that the BJT transistor in figure 9 is operating in the saturation region, then the threshold voltage between bas $B$ and emitter $E$ is $\mathrm{V}_{\mathrm{BE}}=0.8 \mathrm{v}$ and the voltage between collector C and emitter $E$ is $V_{C E}=0.2 \mathrm{v}$. This paper follows the circuit $\theta \rightarrow \mathrm{B} \rightarrow \mathrm{E} \rightarrow \mathrm{g}$ and obey the Kirchhoff's voltage law to calculate the current.

$$
\begin{aligned}
& V_{6}-I_{B} R_{B}-V_{B E}-I_{C} * 0.2 K \Omega=0 \\
\Rightarrow \quad & 13-I_{B}^{*} 5 K \Omega-0.8-I_{C}^{*} 0.2=0-----2
\end{aligned}
$$

(5) In figure 9, follow the loop $\mathrm{d} \rightarrow \mathrm{e} \rightarrow \mathrm{C} \rightarrow \mathrm{E} \rightarrow \mathrm{g}$ and obey the Kirchhoff's voltage law to calculate the current $\mathrm{I}_{\mathrm{C}}$.

$$
V_{C C}-I_{C} * 1 \mathrm{k} \Omega-V_{C E}-I_{C} * 0.2 K \Omega=0
$$

$\Rightarrow 13 \mathrm{v}-\mathrm{I}_{\mathrm{C}}^{*}(1+0.2) \mathrm{K} \Omega-0.2 \mathrm{v}=0-------8$
$\Rightarrow I_{C}=10.67 \mathrm{~mA}$
$--\Phi$
In the calculation process of formula $\Theta, 1 \mathrm{~K} \Omega$ is an approximate value representing the impedance of the induction coil inside the relay. Substitute equation $\Phi$ into $\otimes$ to calculate the current $\mathrm{I}_{\mathrm{B}}$ :

```
13-IB*5-0.8-10.67*0.2=0
=> IB}=2m
-- -
```

(6) Because of $\left(\mathrm{I}_{\mathrm{C}}=10.67 \mathrm{~mA}\right)<\left(\beta \mathrm{I}_{\mathrm{C}}=150 * 2=300 \mathrm{~mA}\right)$, therefore it can be confirmed that the BJT transistor is operating in the saturation region and the previous assumption $\mathrm{V}_{\mathrm{BE}}=0.8 \mathrm{v}$ is correct.
(7) The function of the BJT transistor in figure 9 is similar to an electronic switch. When the BJT transistor is turned on, then the collector current $I_{C}$ starts to flow (Assume that the current $\mathrm{I}_{\mathrm{C}}$ through the collector is approximately equal to the current $I_{E}$ through the emitter E). Although there will be some errors in such assumptions, but these errors are tolerable.
(8) The relay in figure 9 has been routed. Because the $I_{C}$ current passes the internal electric induction coil to generate magnetism and attracts the H -shaped cast iron to the ca end, therefore the ca end can be current. Because the ca terminal can pass the current, therefore the right side of the relay becomes a closed loop. The AC power can enter the AC motor completely to make the motor run. A diode is connected to the outside of the relay to protect the coil from the reverse flow of $I_{C}$ current.

## VIII. The experiment data (The truth table)

## Table 1. The truth table

| selection of SW1 | selection of freguency | selection of SW2 | state of motor | the number displayed on the LED | time of operation |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $555$ <br> oscillator | $\begin{gathered} \mathrm{f}=1 \mathrm{~Hz} \\ \text { (fixed) } \end{gathered}$ | up | running | 7,8,9,10,11,12,13 | 7 (sec) |
|  |  |  | stop | 14,15,0,1,2,3,4,5,6 | 9 (sec) |
|  |  | down | running | 7,6,5,4,3,2,1,0,15 | 9 (sec) |
|  |  |  | stop | 14,13,12,11,10,9,8 | 7 (sec) |
| function generator (F.G.) | $\begin{gathered} f_{1}=0.5 \mathrm{~Hz} \\ \left(T_{1}=2 \mathrm{sec}\right) \end{gathered}$ | up | running | 7,8,9,10,11,12,13 | 14 (sec) |
|  |  |  | stop | 14,15,0,1,2,3,4,5,6 | 18 (sec) |
|  |  | down | running | 7,6,5,4,3,2,1,0,15 | 18 (sec) |
|  |  |  | stop | 14,13,12,11,10,9,8 | 14 (sec) |
|  | $\begin{aligned} & \mathrm{f}_{2}=0.667 \mathrm{~Hz} \\ & \left(\mathrm{~T}_{2}=1.5 \mathrm{sec}\right) \end{aligned}$ | up | running | 7,8,9,10,11,12,13 | 10.5 (sec) |
|  |  |  | stop | 14,15,0,1,2,3,4,5,6 | 13.5 (sec) |
|  |  | down | running | 7,6,5,4,3,2,1,0,15 | 13.5 (sec) |
|  |  |  | stop | 14,13,12,11,10,9,8 | 10.5 (sec) |
|  | $\begin{gathered} \mathrm{f}_{3}=1.25 \mathrm{~Hz} \\ \left(\mathrm{~T}_{3}=0.8 \mathrm{sec}\right) \end{gathered}$ | up | running | 7,8,9,10,11,12,13 | 5.6 (sec) |
|  |  |  | stop | 14,15,0,1,2,3,4,5,6 | 7.2 (sec) |
|  |  | down | running | 7,6,5,4,3,2,1,0,15 | 7.2 (sec) |
|  |  |  | stop | 14,13,12,11,10,9,8 | 5.6 (sec) |

IX. The photo. of completed device


Fig. 10 The photo. of completed device

## X. Conclusion

(1) There is a resistance of $200 \Omega$ between the emitter (E) and ground ( g ) of the BJT transistor in figure 8 and figure 9. The resistance of $200 \Omega$ is regarded as a current limiting resistance to present excessive current from passing through the BJT transistor and burn down the transistor.
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