Journal of Multidisciplinary Engineering Science and Technology (JMEST)
ISSN: 2458-9403
Vol. 10 Issue 10, October - 2023

Timed Oscillating Alarm System

Shih-Ping Hu
Department of Civil engineering
Hungkuo Delin University of Technology
New Taipei City, Taiwan, Republic of China
hushihping@yahoo.com.tw

Abstract--Because of the evil of human nature and the greed of human nature, the problem of law and order is endless in the modern society. Therefore, the time alarm system is the best weapon for the security enterprise. The security guard sets the time for the protection of a valuable custody (name painting, jewelry, gold, diamonds, jade, etc.). When the time of the timer reaches the set quarantine time, the arm will flash continuously. In this way, the security guard can be reminded to pay attention to safety and avoid thieves' invasion.

Timed oscillating alarms can also be used for military purpose. At the time of the war between the two armies, the combatant commanders send the troops to different positions according to different operational tasks. The combat commander sets a time (t_s) and starts timing (t). When the timing time (t) reaches the attack time (t_s), the alarm emits a flashing signal and each combat group simultaneously attacks to destroy the enemy.

Keywords—8-bit magnitude comparator, astable multistage oscillator, modulus 100up counter, 4-bit magnitude comparator

I. INTRODUCTION

This paper can be divided into five parts. The first part is the setting of the alarm time [t_s(sec)]. The encoder is used to input the decimal timing seconds [t_s(sec)] into the encoder to compile the digital code into the 8-bit magnitude comparator. At the same time, the timing seconds [t_s(sec)] will be displayed on the 7-segment LED display. The second part is the 555 astable multistage oscillator. A digital pulse will be sent every second to stimulate the subsequent modulus 100 up counter. The third part is the modulus 100 up counter. The modulus 100 up counter is used to calculate the instantaneous seconds [t (sec)]. The fourth part is the 8-bit magnitude comparator that is composed by two 4-bit magnitude comparators (two logic IC 7485). The 8-bit magnitude comparator is used to compare whether instantaneous seconds [t (sec)] exceeds timing seconds [t_s(sec)] or not. The fifth part is alarm system. When the instantaneous second [t(sec)] reaches the timing second [t_s(sec)], then the alarm system is started.

II. LITERATURE REVIEW

There are some examples for the research on the timed burglar alarm system in previous years. In the literature [1], professor Wang Zhihao studied and designed the most basic "car burglar alarm". The advantage of this paper is that the construction is simple and the cost is low. The disadvantage is that it can only be applied in the car. In the literature [2], Mr. Liu Liangyong researched and designed the "exquisite car burglar alarm". The advantage of this paper compared with the literature [1] is that it is simpler and cheaper to construct. The disadvantage of this paper is that it is too fine to make the owner misunderstand.In the literature [3], professor Shi songcun researched and designed "HOL TEK home security burglar alarm". The advantage of this paper is that it is very extensive and practical in daily home life. The disadvantage of

this paper is that there are many sensors. If only as one of these sensors is faulty, the system will be distorted. In the literature [4], Mr. Chen Yanxu researched and designed “the simple and easy to use electronic time switch”. The advantage of this paper is that it is very simple and easy to use. The disadvantage of this paper is that the function generator is still used in this paper and the degree of the innovation is insuffient.

III. PRINCIPLE EXPLANATION

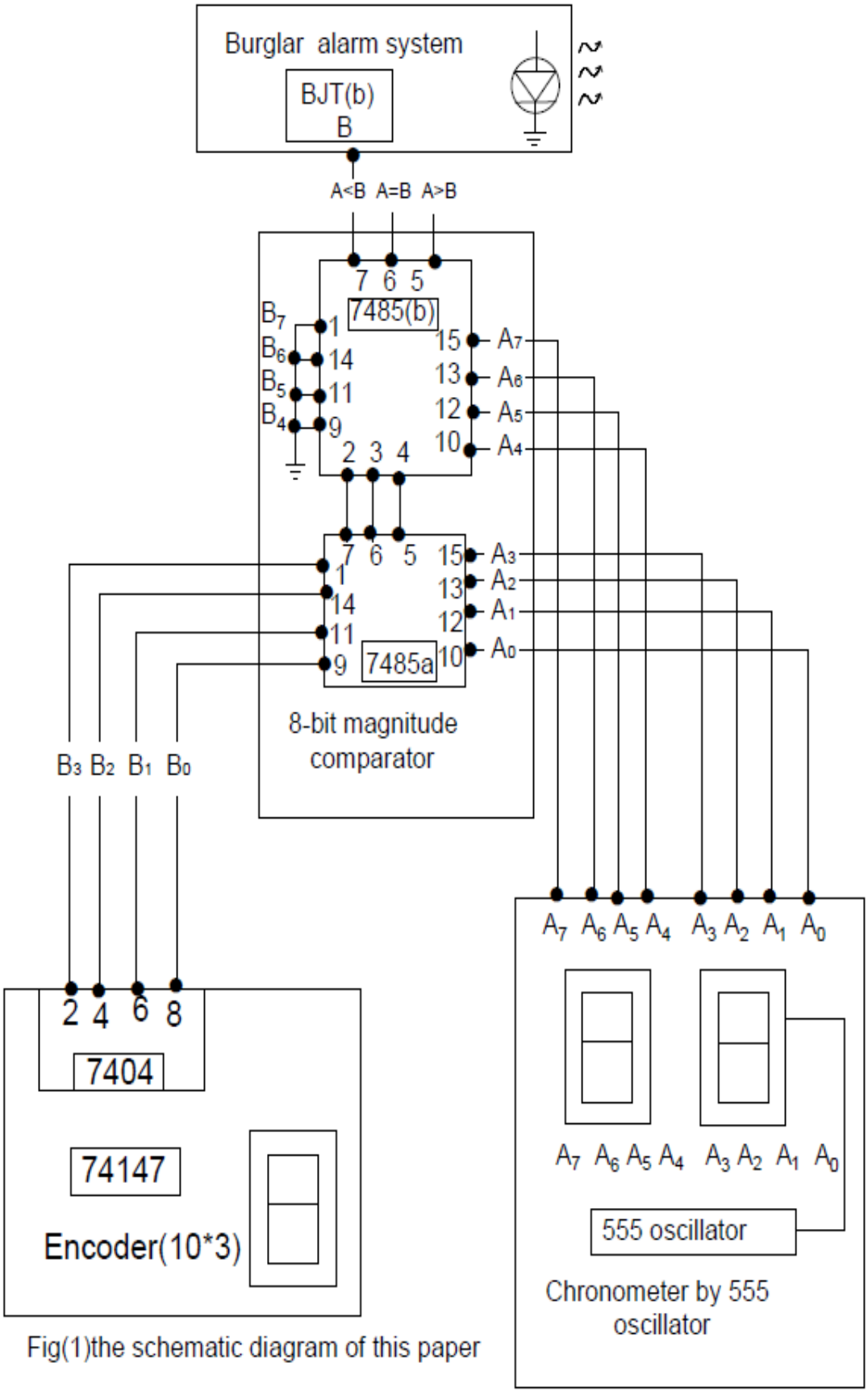
(1) The electronic component used in this paper are counted as ①logic IC 7490*2, 7447*3, 74147*1, 7404*2, 7400*1,7485*2 ②analog IC 555*2 ③npn type BJT transistor*2 ④ LED light*1 ⑤ common-anode 7-segment LED display ⑥ resistance (1/4 w): 200Ω * 23, 1kΩ * 2, 2.2kΩ * 2, 5kΩ * 2, 10kΩ * 1, ⑦capacitance (50w): 0.001μF * 1, 100μF * 2, ⑧diode (numbering IN4001) * 1, ⑨circuit strip (numbering: EIC-108) * 1

(2) The wiring diagram of this paper is shown in Figure (1) ~ Figure (5). Figure (1) is a schematic diagram of the overall circuit. Figure (2) is the wiring detail of the encoder (10X3). Figure (3) is the wiring detail of the chronometer by the 555 astable multistage oscillator. Figure (4) is the detailed wiring diagram of 8-bit magnitude comparator. Figure (5) is the detailed wiring diagram of the burglar alarm system.

(3) In figure (2), D_1~D_9 represent the number of seconds (t_s) to be set in this paper. For example: if we need to set t_s=9(seconds), we need to connect D_9 to high potential / (5V) shown as figure (6).The t_s =9 is encoded into a binary code “$B_3B_2B_1B_0$=/ØØ/$_{(2)}$” through logic IC 74147 and output from 16,6,7,9 pin. The digital code $B_3B_2B_1B_0$= /ØØ/$_{(2)}$ cannot be understood by human and it must be translated to the number “9” that can be understood by human through logic IC7404(a) and 7447(c) and display on the 7-segment

LED display (c) shown as figure (6).

(4) In figure (3), the 555 astable multistage oscillator is a circuit that is mixed and combined by the analog circuit and the digital circuit. It is commonly used in time control (delay time) and digital pulse generation. The most important effect is that it can replace the traditional function generator, anyway, it can reduce the dependence on the function generator at least.



Fig(1)the schematic diagram of this paper

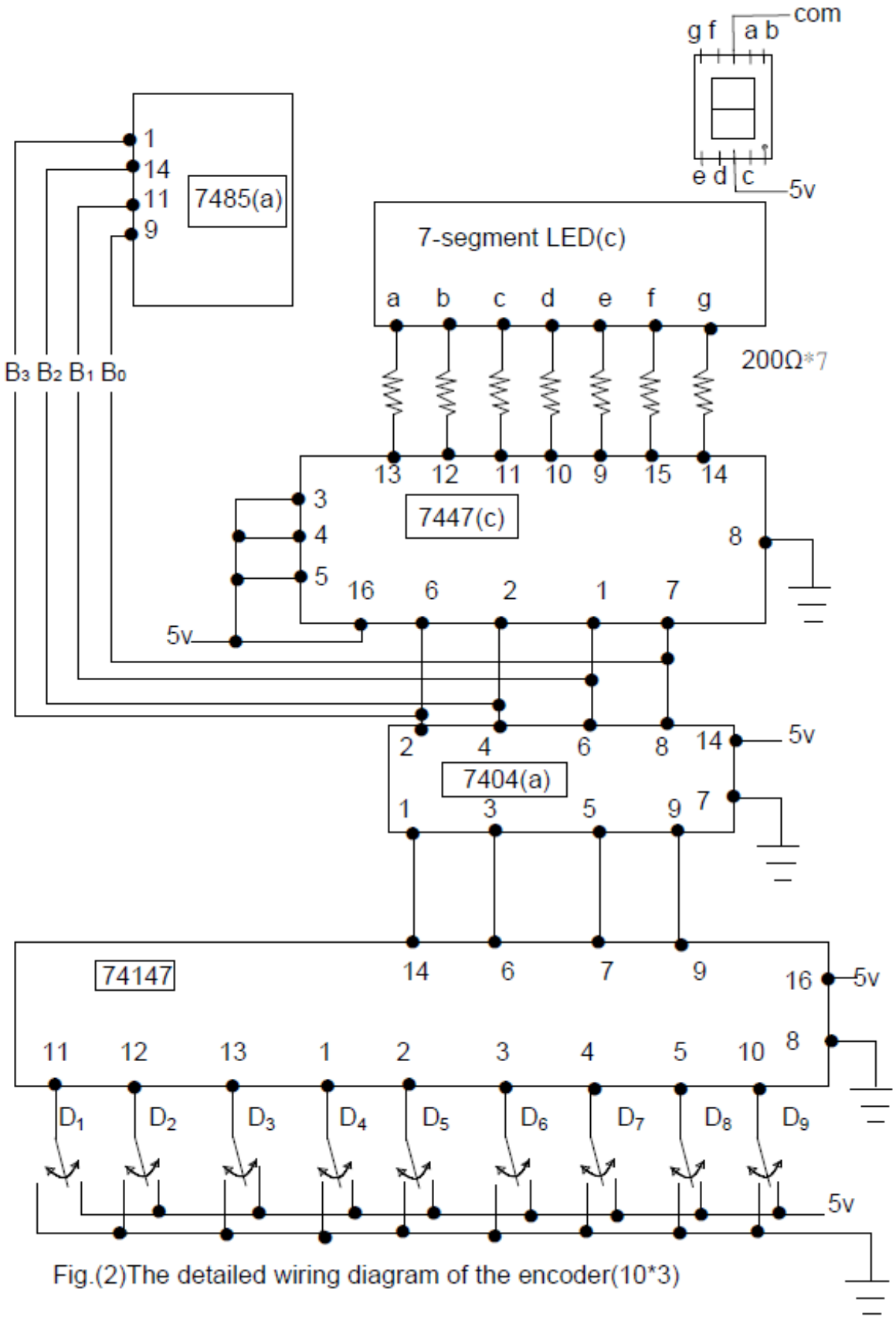


Fig.(2)The detailed wiring diagram of the encoder(10*3)

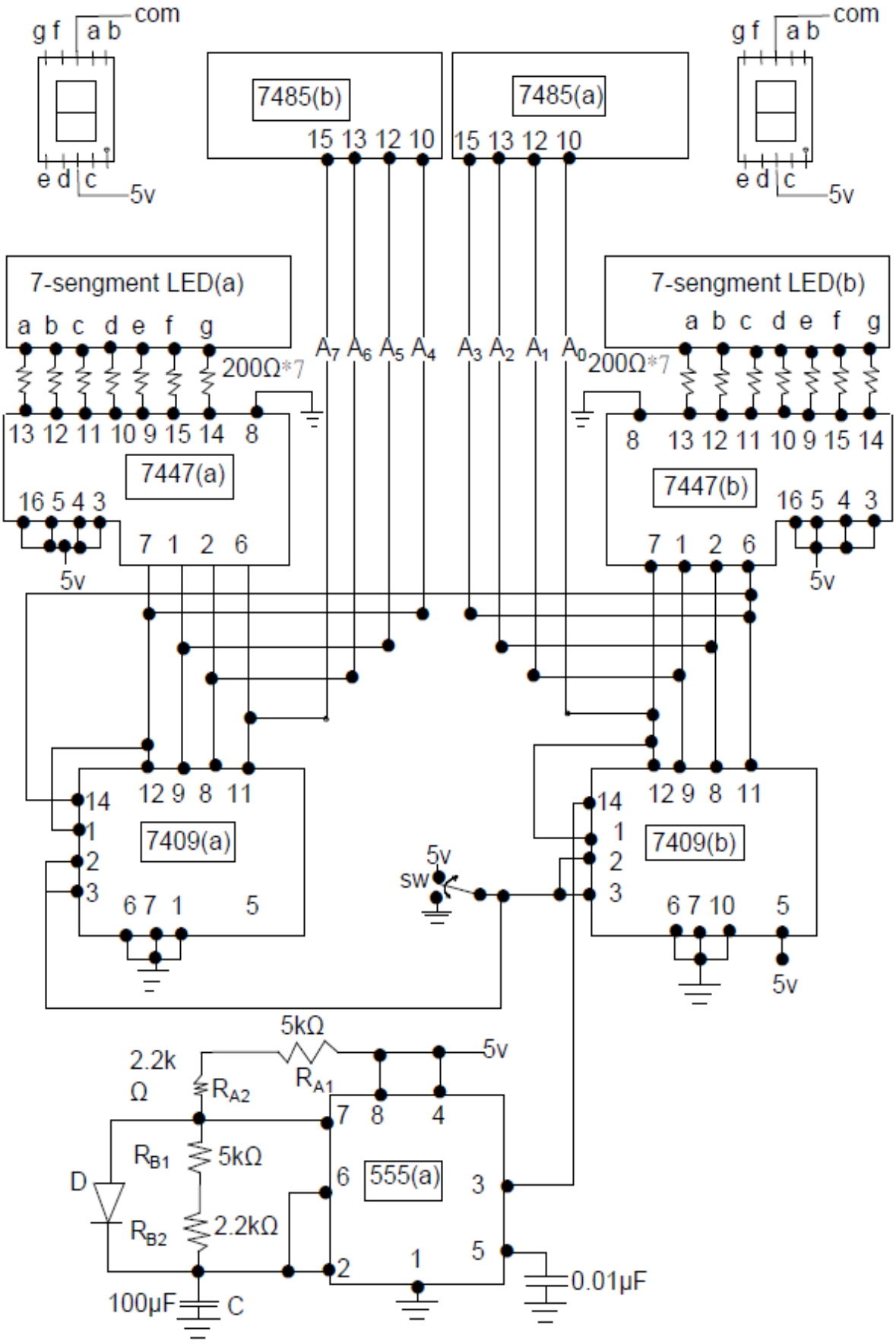


Fig.(3)The detailed wiring diagram of the chronometer by 555 oscillator

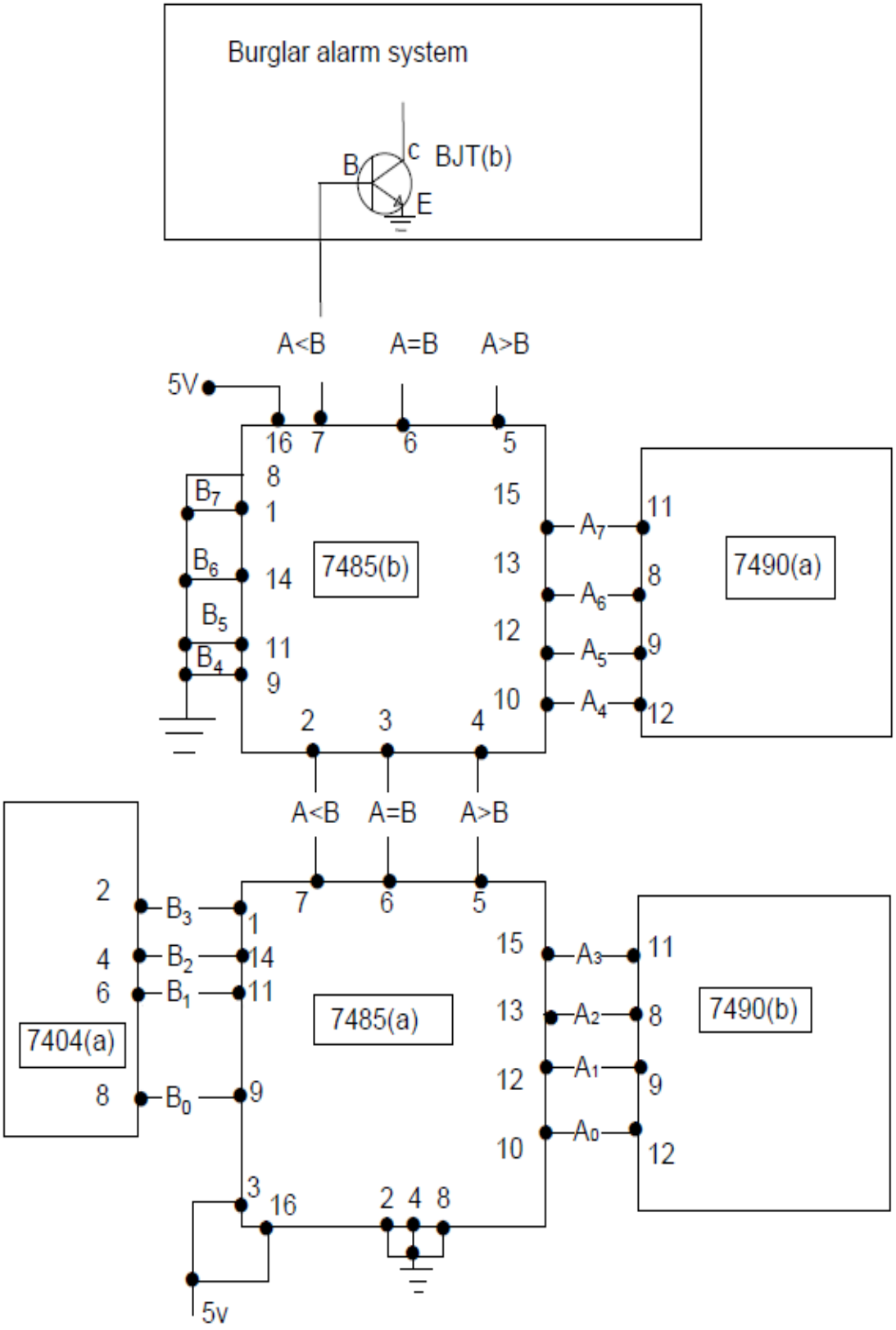


Fig.(4)The detailed wiring diagram of 8-bit magnitude comparator

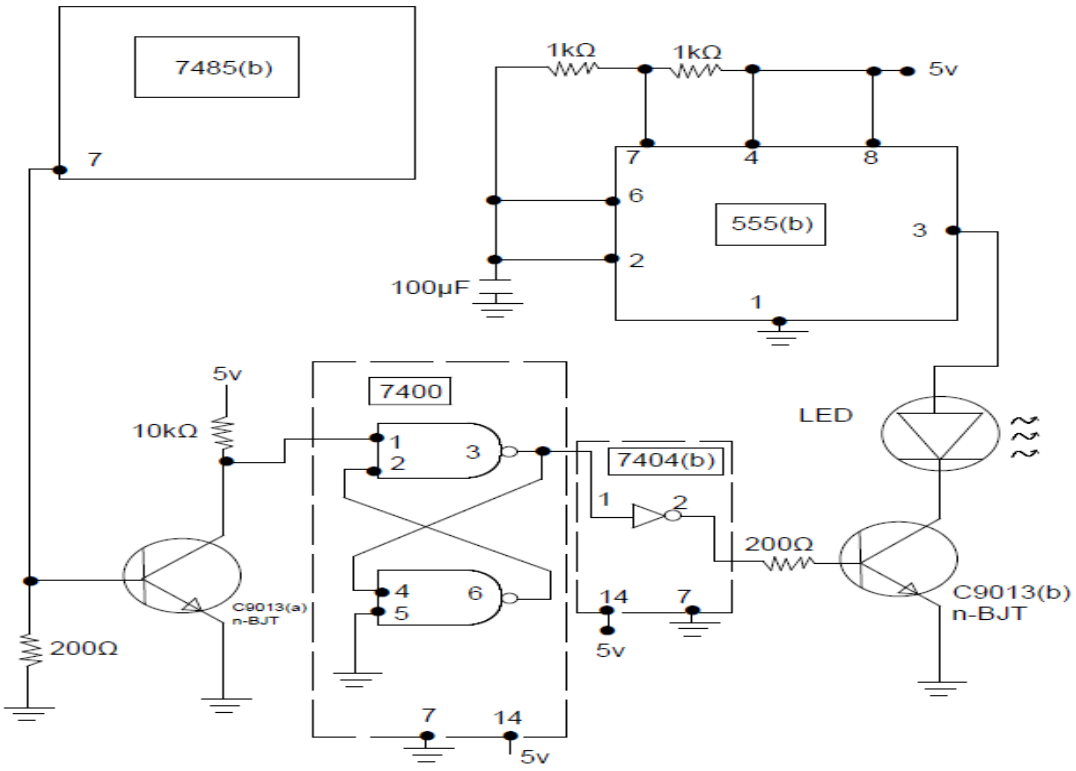


Fig.(5)The detailed wiring diagram of buglar alarm system

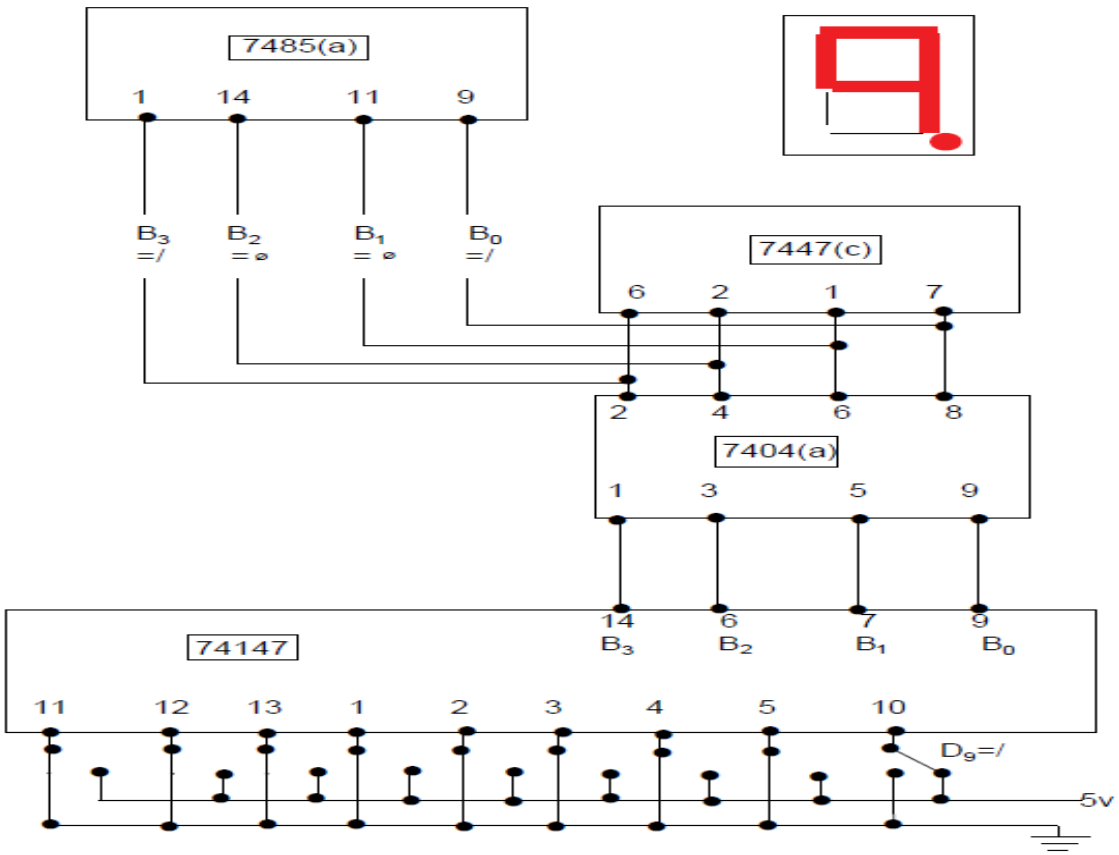


Fig.(6)The logic detailed diagram of the encoder(10*3)
in the case of D_9=/(t_s=9sec)

IV. THE PRINCIPLE OF 555 ASTABLE MULTISTAGE OSCILLATOR

(1) In figure (7), the folding line represents the route that the current travels during the first charging of 555 oscillator. The current flows from point a through R_A resistance to point b. On the b-point, because the internal resistance R_D of the diode itself is only about 5Ω is much smaller than $R_B=R_{B1}+R_{B2}=7.2K\Omega$, therefore the current all pass through the b-d-e-f-g route without passing through the R_B resistance. At the same time, the output voltage of the 555 oscillator ($V_3=V_{out}$) is the DC bias (V_{CC}) (ie, $V_{out}=V_3=V_{CC}=5V$). Because figure (7) is the first charge, the time it used is transient and is denoted by t_0.

(2) In figure (8), the folding line represents the path that the current travels during the discharging of the 555 oscillator. The current starts from point g and arrives to point f. At the point f, the current cannot enter the f-e-d segment because of the reverse action of the diode itself. At the point f, the only choice of the current path is to pass through the R_B resistance and enter the 555oscillator by the 7th pin of the 555 oscillator. At the same time, the output voltage $V_3(V_{out})$ is low potential ($V_3=V_{out}=0V$). The time required for this discharging is t_1 (sec).

(3) In figured (8), the time required for the discharging can be calculated as follows that is based on the resistance R_B passed through the discharging path (g→ f→ b→ pin7)

$t_1=R_B*C*\ln 2=(7.2X10^{3\Omega})*(100X10^{-6}F)*\ln 2=0.5(sec)$

(4) In figure (9), the charging time required t_2(sec) after the second charging can be calculated as follows that is based on the charging path (a→b→ d→ e→ f→ g) after the second charging in figure (9). (neglecting the internal resistance of the diode $R_D=5\Omega$)

$t_2=R_A*C*\ln 2=(70.2X10^{3}\Omega)*(100X10^{-6}F)*\ln 2=0.5$ (sec)

(5) The output pulse of the 555 oscillator after the second charge is shown in figure (10). Except for the astable of the first charge, the period of the remaining pulse waves is 1 second (T=1 sec) and the frequency is 1 Hz (f=1/T= 1/1sec= 1 Hz)

(6) Connect the output pulse (digital pulse) of figure (10) to the 14^{th} of logic IC 7490(b) in figure (3) as the input pulse of IC 7490(b) (negative edge-triggered)

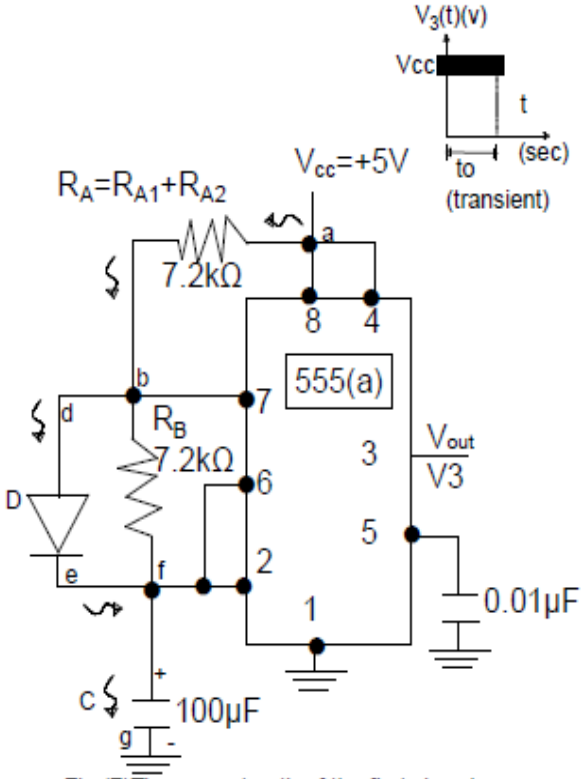


Fig.(7)The current path of the first charging

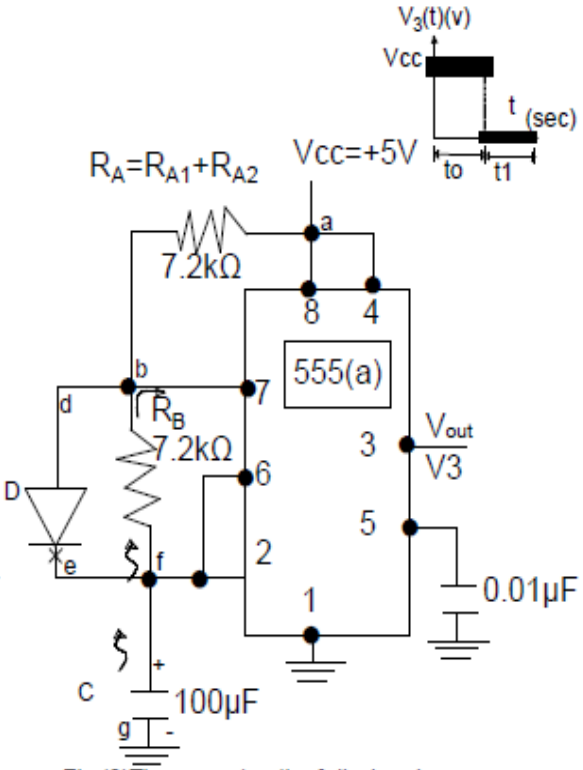


Fig.(8)The current path of discharging

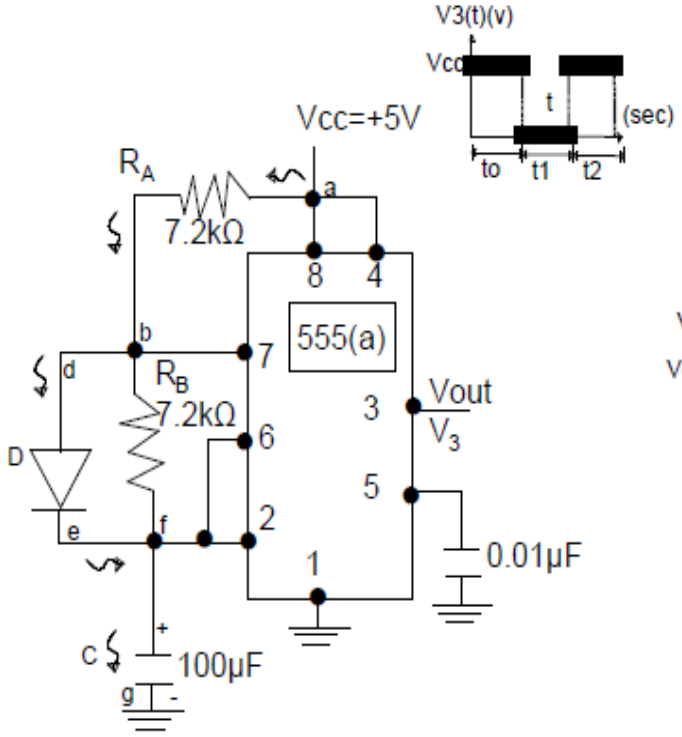


Fig.(9)The current path of the second charging

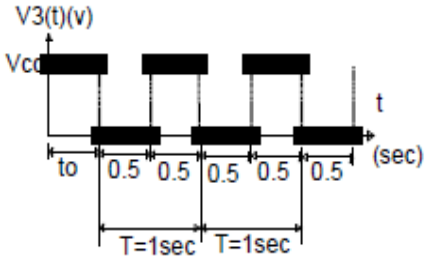


Fig.(10)The overall output pulse of 555 oscillator

V. THE PRINCIPLE OF MODULUS 100UP COUNTER BY 555 OSCILLATOR

(1) When SW=/ (high potential), then logic IC 7490(b) and 7490(a) are all cleared. The logic diagram is shown as figure (11). When SW=/(high potential), this is the zeroing action of the chronometer. Although the digital pulse of the 555 oscillator continues to pass to CK(b), it still cannot excite IC7490(b). At this time, the display is 00

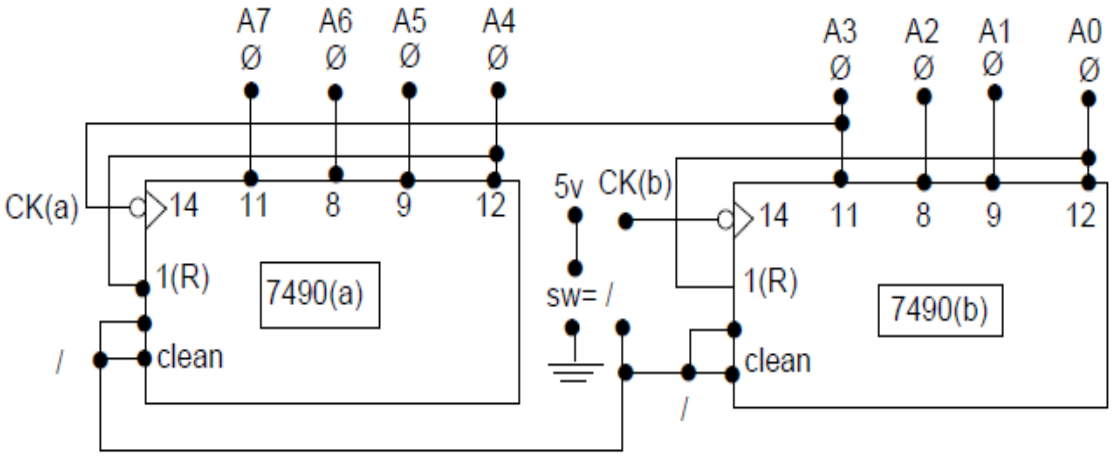
(2) When SW=Ø (low potential), the condition before the 100th trigger of CK(b) is shown as figure (12) and the display is 99.

(3) When SW=Ø (low potential), the first temporality after the 100th trigger at CK(b) is shown as figure(13). Because IC7490(b) is reset, it causes A_3:/→Ø and A_0:/→Ø. At the same instant, because A_3:/→Ø causes CK(a):/→Ø(negative edge
-triggered) and the display is 90.

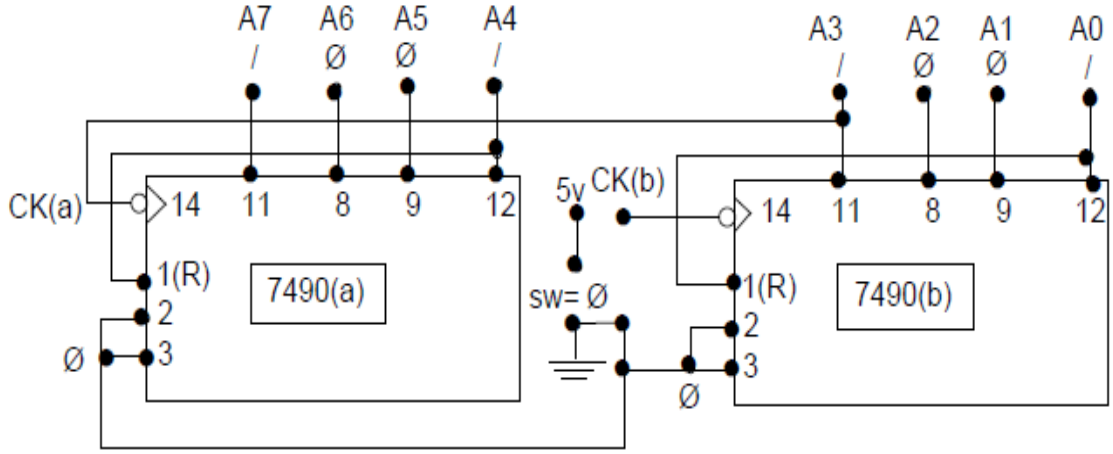
(4)When SW=Ø (low potential), the second temporality after the 100th trigger at CK(b) is shown as figure(14). Because CK(a):/→Ø (negative edge-triggered), it causes IC7490(a) enter a decimal that is A_5:Ø→/ and A_4:/→Ø.

(5) When SW=Ø (low potential), the third temporality after the 100th trigger at CK(b) is shown as figure(15). Because A_4:/→Ø is fed back to the first pin of the IC7490(a), Pin 1 is turned to Ø (low potential) and IC7490(a) is reset.

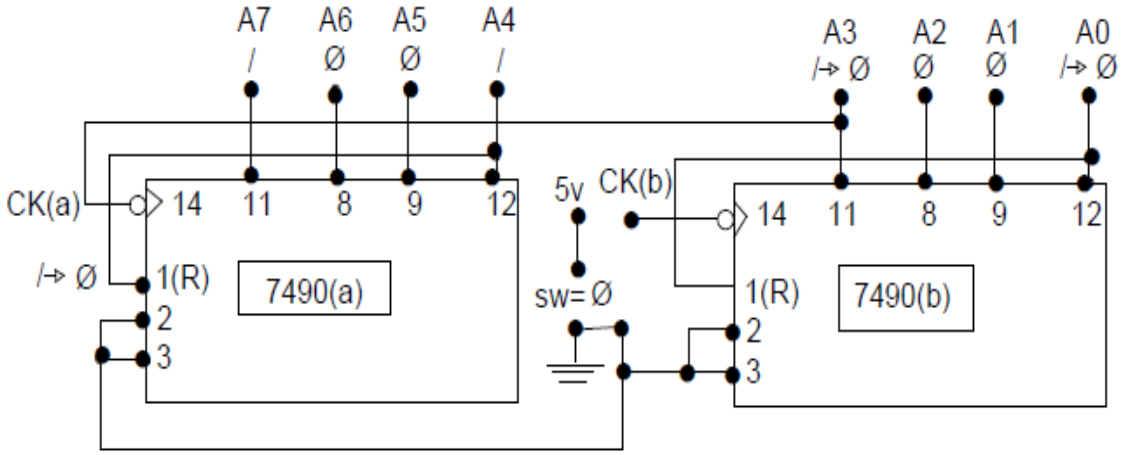
(6) When SW=Ø (low potential), the fourth temporality after the 100th trigger at CK(b) is shown as figure (16). Because IC7490(a) is reset, it causes $A_7A_6A_5A_4$= ØØØØ$_{(2)}$ and the display is 00



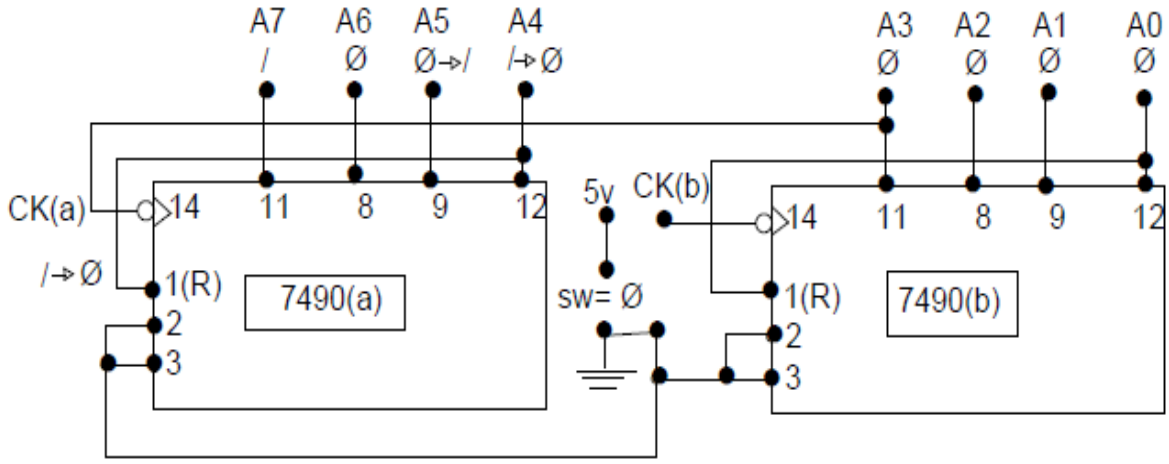
Fig(11) the logic diagram for the case of sw=/(5v)



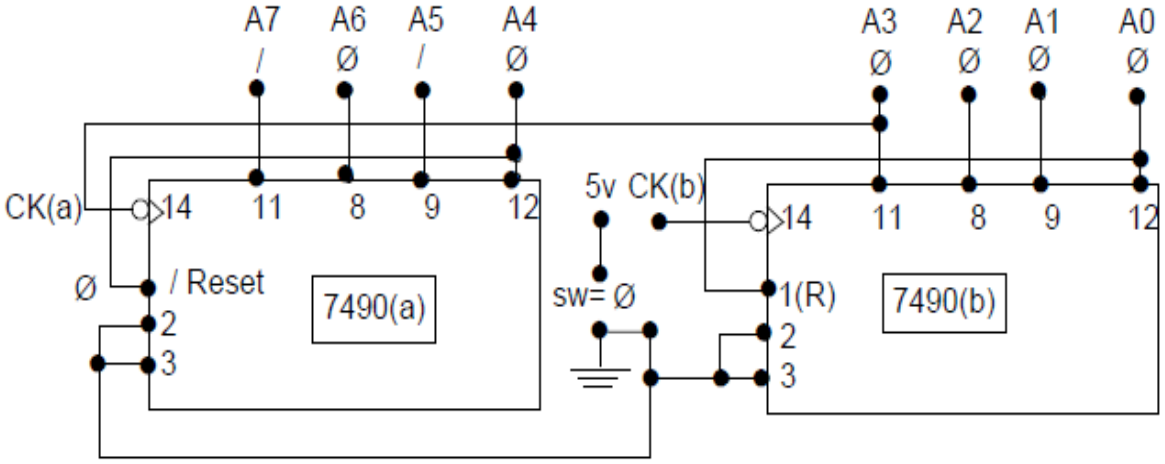
Fig(12) the logic state before the 100th trigger at ck(b)



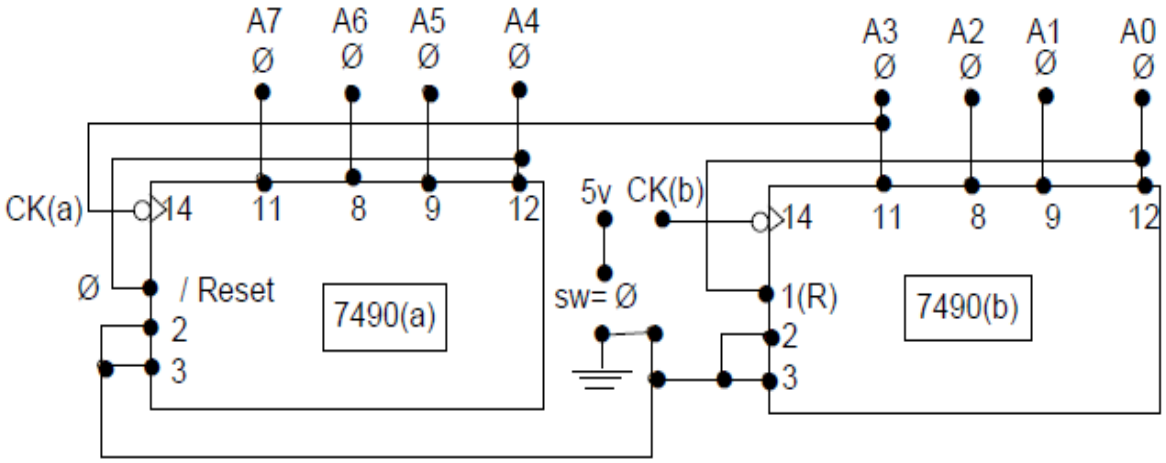
Fig(13) the first temporality after the 100th trigger at ck(b)



Fig(14) the second temporality after the 100th trigger at ck(b)



Fig(15) the third temporality after the 100th trigger at ck(b)



Fig(16) the fourth temporality after the 100th trigger at ck(b)

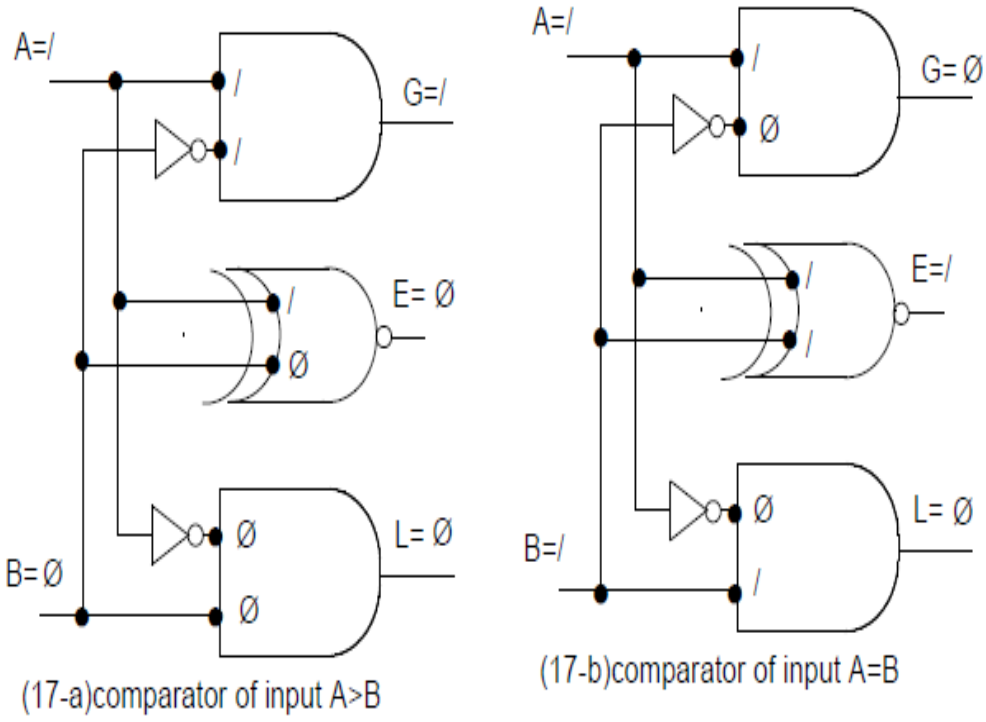
VI. THE PRINCIPLE OF 8-BIT MAGNITUDE COMPARATOR

(1) Figure (17) is a logic diagram of a 1-bit magnitude comparator. When A>B is input, the output will be G=/ and E=Ø and L=Ø as shown in figure (17-a). When A=B is input, the output will be G=Ø and E=/ and L=Ø as shown in figure (17-b, c). When A<B is input, the output will be G=Ø and E=Ø and L=/ as shown in figure (17-d).

(2) Figure (18~20) is a 2-bit magnitude comparator that is composed of two 1-bit magnitude comparators. When A>B is input, the output will be G=/ and E=Ø and L=Ø as shown in figure (18). When A=B is input, the output will be G=Ø and E=/ and L=Ø as shown in figure (19). When A<B is input, the output will be G=Ø and E=Ø and L=/ as shown in figure (20).

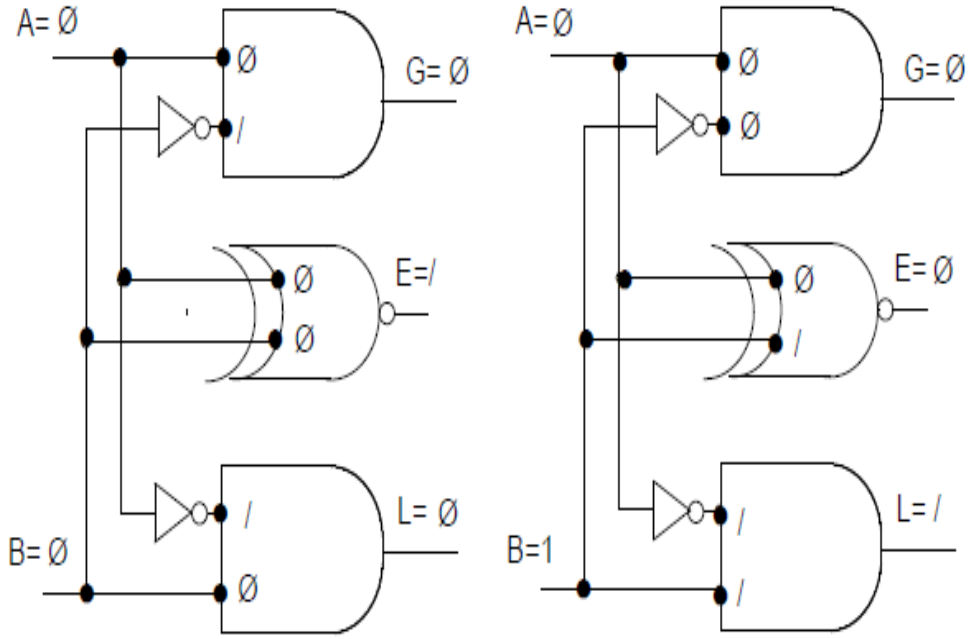
(3) Figure (21~23) is a 4-bit magnitude comparators that is composed of two 2-bit magnitude comparators. When A>B is input, the output will be G=/ and E=Ø and L=Ø as shown in figure (21). When A=B is input, the output will be G=Ø and E=/ and L=Ø as shown in figure (22). When A<B is input, the output will be G=Ø and E=Ø and L=/ as shown in figure (23).

(4)The same reason can be proved that two 4-bit magnitude comparators can be combined into an 8-bit magnitude comparator as shown in figure (4). When $A_7A_6A_5A_4A_3A_2A_1A_0<B_7B_6B_5B_4B_3B_2B_1B_0$ is input, the output will be G=Ø and E=Ø and L=/ [the seventh pin of 7485(b) is high potential / (the output voltage is almost 4.8 V).]. When $A_7A_6A_5A_4A_3A_2A_1A_0>B_7B_6B_5B_4B_3B_2B_1B_0$ is input, the output will be G=/ and E=Ø and L=Ø [the seventh pin of 7485(b) is low potential / (the output voltage is almost 0.1 V)].



(17-a)comparator of input A>B

(17-b)comparator of input A=B

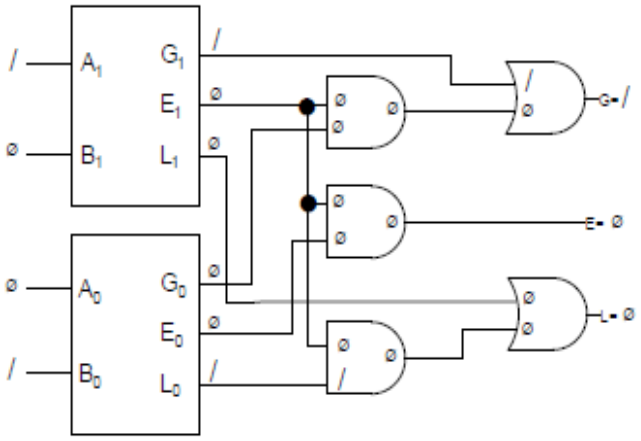


(17-c)comparator of input A=B

(17-d)comparator of input A<B

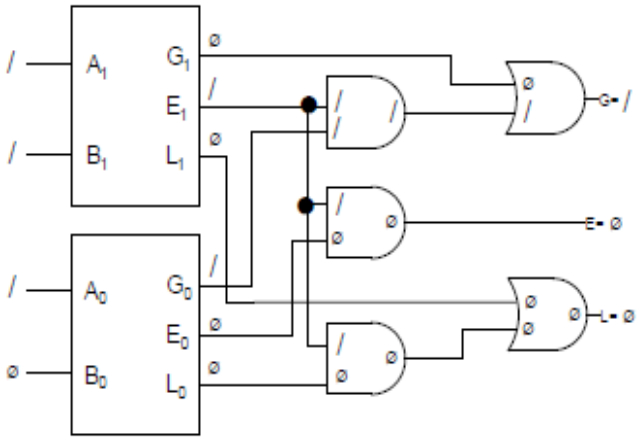
Fig(17)1-bit magnitude comparator

case(1)[A>B]
[A_1A_0= / ø] > [B_1B_0= ø /]



(18-a)input [A_1A_0= / ø] > [B_1B_0= ø /]

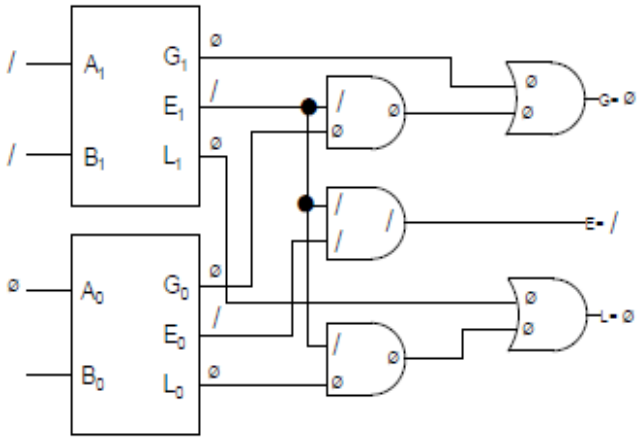
case(1)[A>B]
[A_1A_0= / /] > [B_1B_0= /ø]



(18-a)input [A_1A_0= / /] > [B_1B_0= / Ø]

Fig.(18)2-bit magnitude comparator when the input is A>B

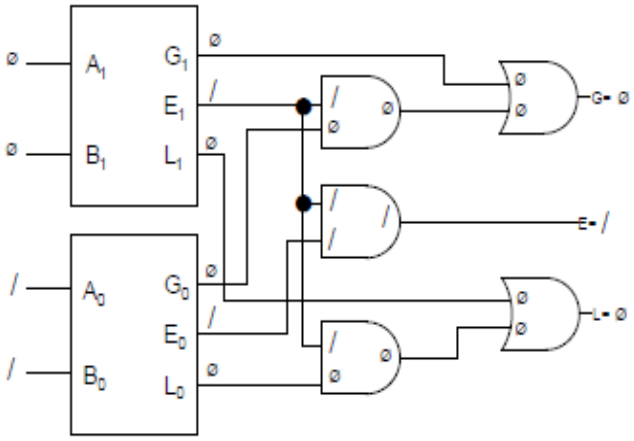
case(2)[A=B]
[A_1A_0= / Ø] = [B_1B_0= / Ø]



(19-a) input [A_1A_0= / Ø]=[B_1B_0= / Ø]

case(2)[A=B]

$[A_1A_0 = ø/\ ] = [B_1B_0 = ø\ /\ ]$

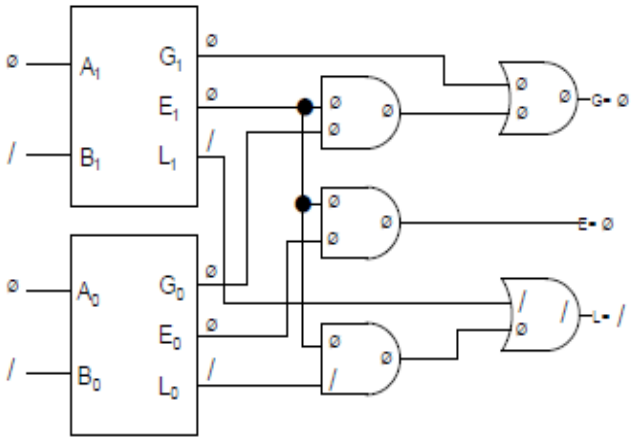


(19-b)input $[A_1A_0 = ø\ /\ ] = [B_1B_0 = ø\ /\ ]$

Fig.(19)2-bit magnitude comparator when the input is A=B

case(3)[A<B]

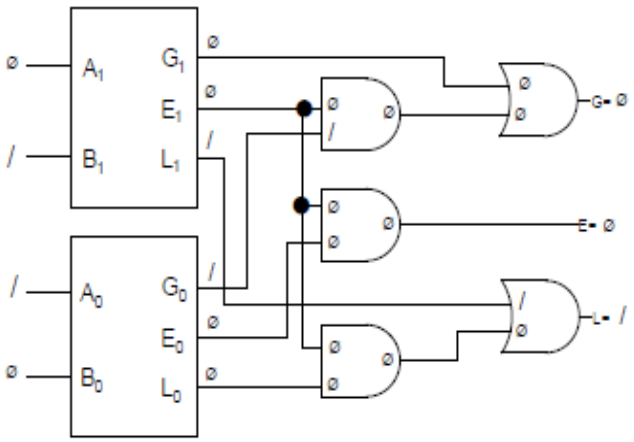
$[A_1A_0 = ø\ ø\ ] < [B_1B_0 = /\ /\ ]$



(20-a)input $[A_1A_0 = ø\ ø\ ] < [B_1B_0 = /\ /\ ]$

case(3)[A<B]

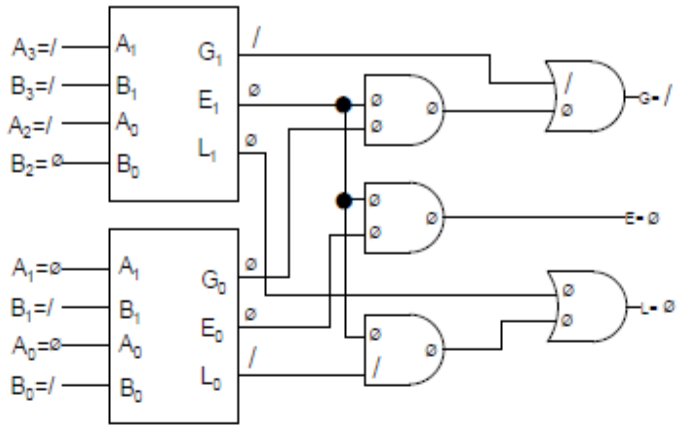
$[A_1A_0 = ø\ /\ ] < [B_1B_0 = /ø\ ]$



(20-b)input $[A_1A_0 = ø\ /\ ] < [B_1B_0 = /ø\ ]$

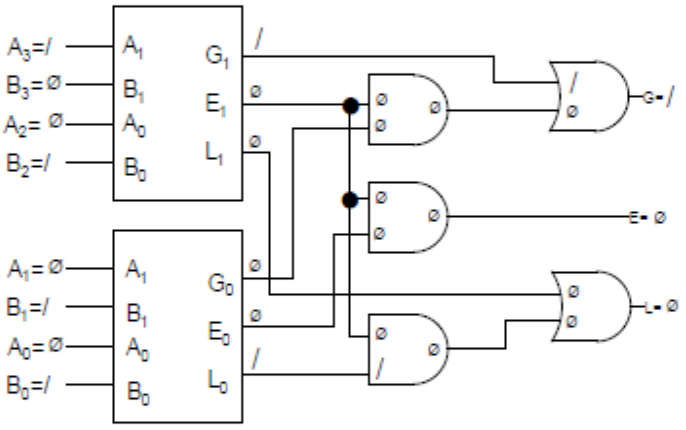
Fig.(20)2-bit magnitude comparator when the input is A<B

case(1)[A>B]
$A_3A_2A_1A_0 > B_3B_2B_1B_0$
//ø ø>/ø//



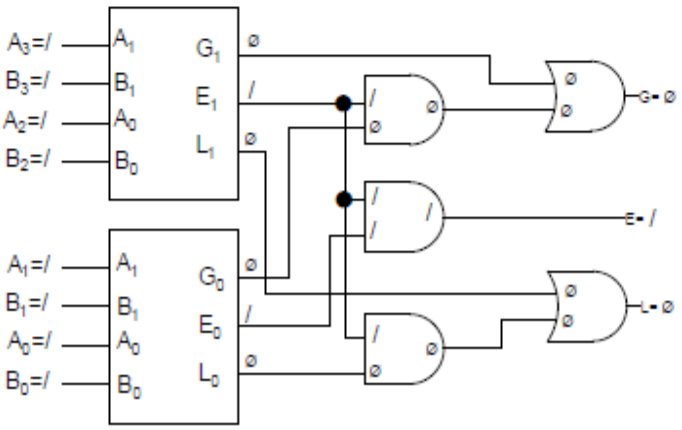
(21-a)input $[A_3A_2A_1A_0 =$ //ø ø$] > [B_3B_2B_1B_0 =$ /ø //$]$

case(1)[A>B]
$A_3A_2A_1A_0 > B_3B_2B_1B_0$
/ø ø ø>ø///



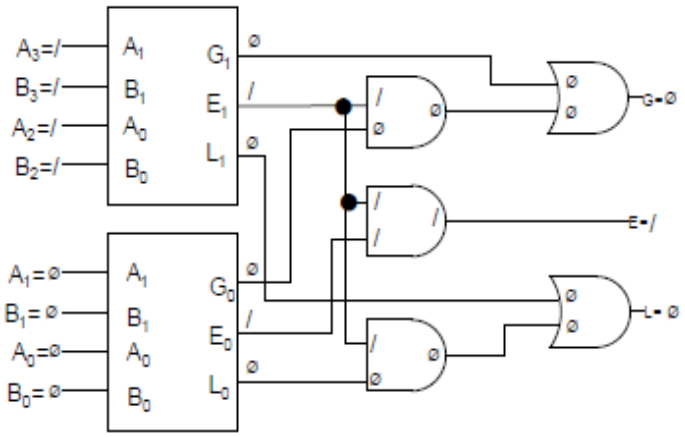
(21-b)input $[A_3A_2A_1A_0 =$ /ø ø ø$] > [B_3B_2B_1B_0 =$ ø / // $]$
Fig.(21)4-bits magnitude comparator when the input is A>B

case(2)[A=B]
$A_3A_2A_1A_0 = B_3B_2B_1B_0$
////=////



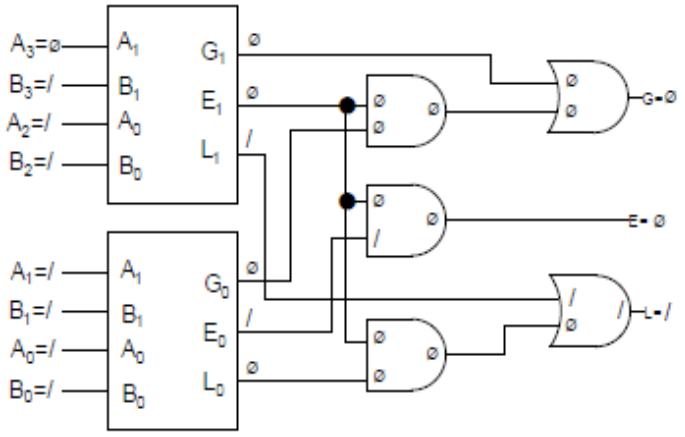
(22-a)input $[\ A_3A_2A_1A_0 =$ ///// $] = [\ B_3B_2B_1B_0 =$ //// $]$

case(2)[A=B]
$A_3A_2A_1A_0=B_3B_2B_1B_0$
//ø ø=// ø ø



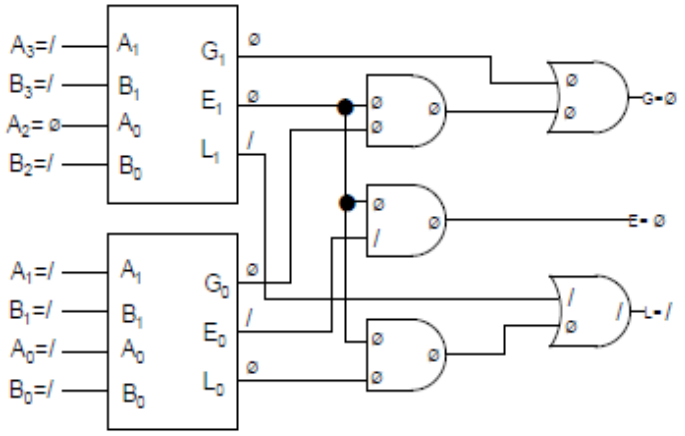
(22-b)input $[A_3A_2A_1A_0 = / / ø ø\ ] = [B_3B_2B_1B_0 = / / ø ø\ ]$
Fig.(22)4-bit magnitude comparator when the input is A=B

case(3)[A<B]
$A_3A_2A_1A_0<B_3B_2B_1B_0$
ø///<////



(23-a)input $[A_3A_2A_1A_0 = ø / / /\ ] < [B_3B_2B_1B_0 = / / / /\ ]$

case(3)[A<B]
$A_3A_2A_1A_0<B_3B_2B_1B_0$
/ø//<////



(23-b)input $[A_3A_2A_1A_0 =\ /ø/ /\ ] < [B_3B_2B_1B_0 = / / / /\ ]$
Fig.(23)4-bit magnitude comparator when the input is A<B

VII. THE PRINCIPLE OF THE BURGLAR ALARM SYSTEM

(1) When $A_7A_6A_5A_4A_3A_2A_1A_0$ <$B_7B_6B_5B_4B_3B_2B_1B_0$ (A<B) is input, the seventh pin of IC7485(b) is / (high potential) and it causes the burglar alarm system is stopped (extinguished). The principle is shown in figure (24)

(2)In figure (24), the voltage at the 7th pin of IC7485(b) and B(a) point is about 0.85V higher than the threshold voltage of the npn-type BJT transistor 0.8V [ie (0.85V)>(V_{BE}=0.8V)], so BJT(a) starts running. Since there is a current between the C(a) point and the E(a) point, the voltage at the C(a) point is 0V (low potential). Subsequently, the IC7400 is a NAND-type flip-flop. The low potential Ø of the point C(a) is converted to high potential / by IC7400, and then turned to low potential Ø by the inverting gate of IC7404. Because the voltage at point B(b) is 0V which is much lower than the threshold voltage of the npn-type BJT transistor (0.8V), so the BJT(b) cannot be activated and the LED light is off.

(3)When $A_7A_6A_5A_4A_3A_2A_1A_0$ >$B_7B_6B_5B_4B_3B_2B_1B_0$ (A>B) is input, the seventh pin of IC7485(b) is Ø (low potential) and it causes the burglar alarm system is started (flashing constantly). The principle is shown in figure (25)

(4)In figure (25), the voltage at the 7th pin of IC7485(b) and B(a) point is about 0V lower than the threshold voltage of the npn-type BJT transistor 0.8V [ie (0V) < (V_{BE}=0.8V)], so BJT(a) is off. The C(a) point is /(high potential). The voltage of C(a) point is about 4.5V. The high potential / of C(a) is transferred to the low potential Ø through the IC7400. The output Ø of IC7400 is transferred to the high potential / through the IC7404 (the IC7404 is an inverting gate). The voltage of second pin of IC7404(b) is about 2.64V. Because (2.64V)> (V_{BE}=0.8V), therefore the BJT(b) is turned on. Because the BJT (b) transistor is started, therefore the current I_C can pass the whole BJT (b) transistor and voltages of both C(b) point and E(b) point are about 0V. The voltage of the third pin of IC555(b) will flash between (1.8~2.2)V, so the LED is lighting immediately.

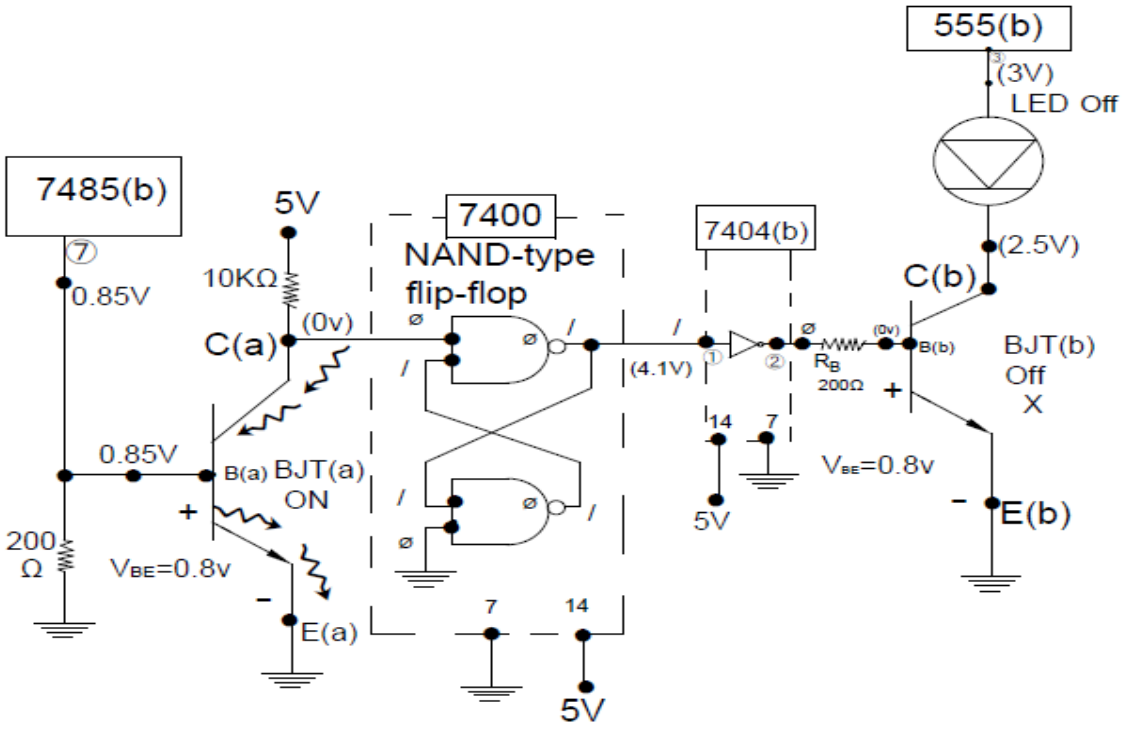


Fig (24)If A is less than B (A<B),the burglar alam system stops(extinguished)

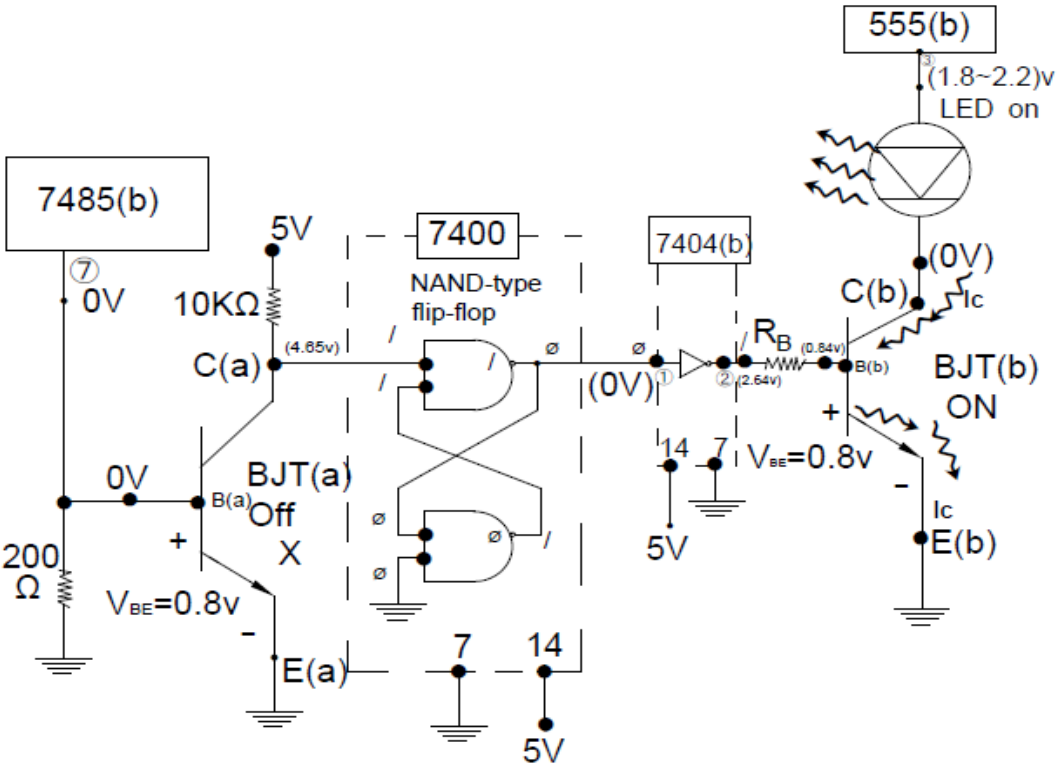


Fig (25)IF A is not less than B (A≥B),the burglar alam system is turned on (flashing)

VIII . PHOTO. COMPLTED (THE TRUTH TABLE)

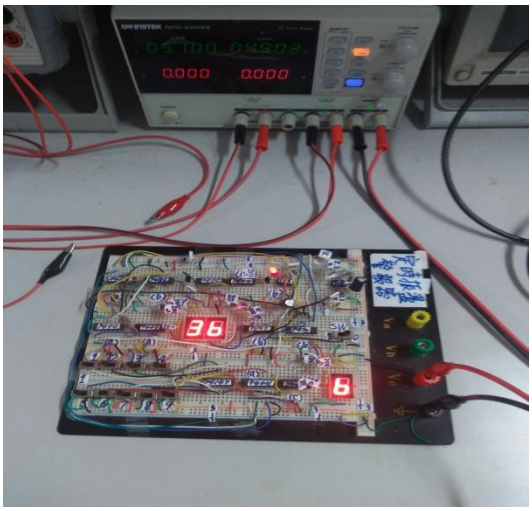


Fig.(26) photo. completed

IX.EXPERIMENT DATA (THE TRUTH TABLE)

Table 1

Selection button	7-segment LED display(c)(delay seconds t_s(sec))	The number of seconds that the burglar alarm
D_1=/	1	1
D_2=/	2	2
D_3=/	3	3
D_4=/	4	5
D_5=/	5	5
D_6=/	6	6
D_7=/	7	7
D_8=/	8	8
D_9=/	9	9

X. CONCLUSION

(1) This paper uses a total of two IC555. The first IC555 is used in the oscillator timer as shown in figure (3). In order to provide the digital pulse of IC7490(b), the resistors $R_A=R_{A1}+R_{A2}=7.2k\Omega$ and $R_B=R_{B1}+R_{B2}=7.2k\Omega$ are deliberately adjusted. The first IC555 is used to replace the traditional function generator, which can reduce the source of error and improve the accuracy of the counting frequency.

(2) The second IC555 is used in this paper is used in the alarm system as shown in figure (5). Adjust the resistance $R_A=R_B=1k\Omega$ in order to provide the pulse wave for LED blinking. The flashing time interval is calculated as follow:

$t_1=t_2=RCln2=(1X10^3\Omega)*(100X10^{-6}F)*(ln2)=0.0693(sec)$

(3) In this paper, the alarm system uses a NAND type flip-flop to provide a stable potential conversion (conversion between high and low potential) to avoid the interference by other electronic components.

REFERENCE

[1]Radio Monthly Magazine (No Wiring Magazine), June 1980, edited by professor Wang Zhihao, “*car burglar alarm*”, page 83~85.

[2]Radio Monthly Magazine(No Wiring Magazine), July 1978, edited by Mr. Liu Liangyong”, *exquisite car burglar alarm*”, page 153~156.

[3]E-Technical Magazine, 38th issue, February 2004, edited by professor Shi Songcun, “*HOL TEK home security burglar alarm*”, page 45~51

[4]E-Technical Magazine (Modern Electronic Publishing House), 186th issue, September 2001, edited by Mr. Chen Yanxu, “*The simple and easy to use electronic time switch*”, page 246~251.

[5]”World TTL/IC specification interchange table”, edited by Quanchua book company, June 2001, page 216, 156, 58, 116, 162.

[6]”*Digital logic design laboratory*”, edited by Mr. Zhang Zhian, Taiwan University of Science and Technology book company, March 2008, page 167~171 and 154~162.