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Time Delay AC Motor

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***Abstract*—Today, when business and industry are very developed, "How do you control your time accurately? " becomes a very important thing. In the process of industrial automation, it is very important to control the start-up time of the motor accurately. We can take some examples to explain why controlling the time accurately is so important. Biochemical plants need to accurately control the capture time of each group of drugs. Start the motor that grabs the arm at the temporality of grabbing time. We use mechanical arms to assemble parts in the automotive industry. We start the motor that grabs the part at the temporality of the setting time (t_s) to assemble the part. In the process control of chemical engineering plant, the timing of starting the motor must be precisely controlled to ensure the correct orientation of the production. If the time of starting the motor can't be well controlled, it will seriously affect the quality. Other applications of time control are numerous.**

Keywords—mechanical arm, process control, 8-bit magnitude comparator.

I. INTRODUCTION

This paper can be divided into five parts. The first part is the setting of the start time (t_S). The decimal delay time [t_S(sec)] is input to the encoder (10X3) and also be displayed on the common anode 7-segment LED display. This encoder is capable of encoding the displayed second (t_S) into binary codes and entering an 8-bit magnitude comparator. The second part is a 555 astable multistage oscillator. The oscillator transmits a digital pulse with a frequency of f=1(Hz) to the subsequent modulus 100 up counter. The third part is the modulus 100 up counter. The modulus 100 up counter is used to calculate the number of seconds in the instant [t (sec)]. The fourth part is an 8-bit magnitude comparator which is composed of two 4-bit magnitude comparators. The 8-bit magnitude comparator is used to compare whether the number of seconds [t(sec)] in an instant exceed the number of seconds of delay [t_S(sec)] or not. The fifth part is the AC motor system. The AC motor system is composed of operational amplifier, relay, diode, npn-type BJT transistor and AC motor. When the instantaneous number of second [t(sec)] reaches the instant of delay time [t_S(sec)] (ie $t \geqq t_S$) the motor starts to run.

II. LITERATURE REVIEW

The research on "time delay AC motor" is represented by the following several papers. In literature [1], professor Li Hongkun studied and designed "AC motor starter and control device". The advantage of this paper is that all analogous electronic components are used, so the structure is simple, but the disadvantage is that the start time cannot be accurately controlled and adjusted. In literature [2], professor Dai Zhengfang researched and designed "stepping motor high-speed operation control circuit". The advantage of this paper is tailor-made for engineering purpose motors. In literature [3], professor

Zhuang Yongyan researches and designs “Combination characteristics of AC motor and variable frequency processor”. In this paper, the fast speed and slow speed of the AC motor depends entirely on the frequency. The advantage is that it can be applied to special medical engineering. The disadvantage is that it can be matched with the feedback control system to achieve the stability requirement. In literature [4], Mr. Xu Maolin researched and designed “AC motor (non-synchronous machine)”. The advantage of this paper is that AC motors can change speed according to different stages of engineering needs, but the disadvantage is that there will be a time delay in the transition of different speeds.

III. PRINCIPLE EXPLANATION

(1) Electronic components used in this paper are ①AC motor (110V, 1/4hp) ②logic IC 7490*2, 7447*3, 74147 *1, 7404*1, 7485*2 ③analog IC 555*1 ④npn-type BJT transistor (C9013)*1 ⑤LED light*1 ⑥common anode 7- segment LED display*3 ⑦resistance(1/4w): 200Ω*22, 2.2KΩ*2, 5KΩ*3, 10KΩ*1, 1KΩ*1 ⑧capacitance(50 w):0.01μF*1, 100μF*1 ⑨diode (numbering:IN4001)*1 ⑩circuit strip (numbering:EIC-108)*1 ⑪relay (numbering: TRD-12VDC -SB- CL) (12V)*3

(2) The wiring diagram of this paper is shown in figure (1) ~ (5). Figure (1) is the schematic diagram of this paper. Figure (2) is the detail wiring diagram of the encoder (10X3). Figure (3) is the detailed wiring diagram of the 555 astable multistage oscillator and modulus 100 up counter, Figure (4) is the detailed wiring diagram of 8-bit magnitude comparator. Figure (5) is the detailed wiring diagram of AC motor system.

(3) D_1~D9 are the delay seconds (t_S) to be set of this paper in figure (2). Let t_S=8 (sec) represent the conversion of D_8 to high potential / (5V) as shown in figure (6). In figure (6), D_8=/ (high potential) is encoded into a binary code (N_3N_2 N_1N_0=/ØØØ$_{(2)}$) by logic IC74147 and then output from the 14th,6th,7th and 9th pins of IC74147. The binary code ($N_3N_2N_1N_0$= /ØØØ$_{(2)}$) cannot be understood by humans. This binary code must be converted to the number “8” that is understood by humans through IC7404 (a) and IC7447(c) and displayed on the 7- segment display(c) as shown in figure (6).

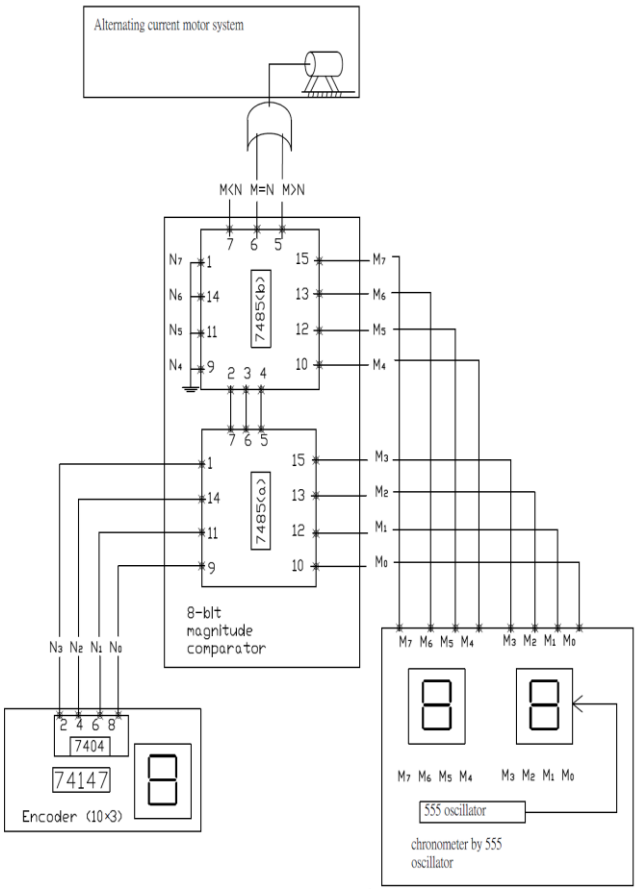


Fig.(1) The schematic diagram of this paper

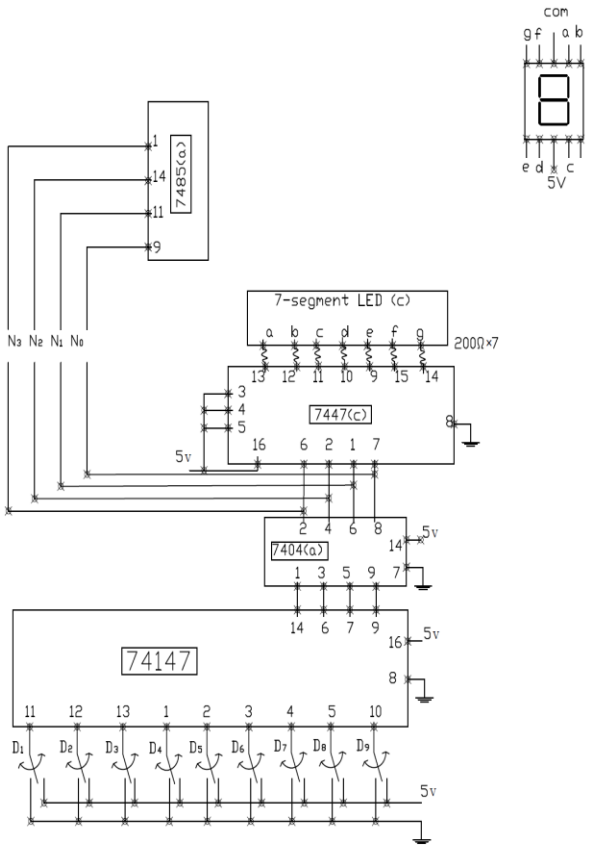


Fig.(2) The detailed wiring diagram of the encoder(10X3)

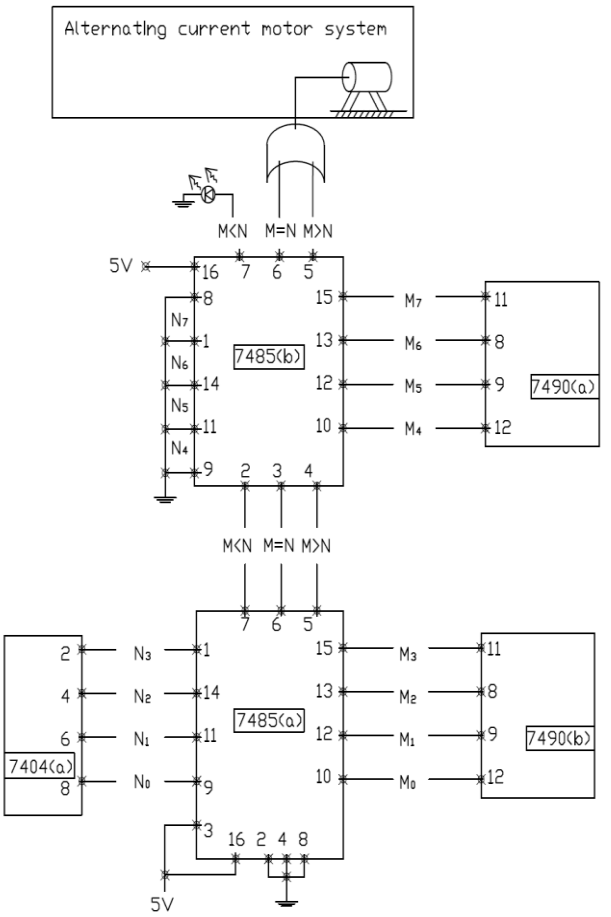


Fig.(4) The detailed wiring diagram of 8-bit magnitude comparator

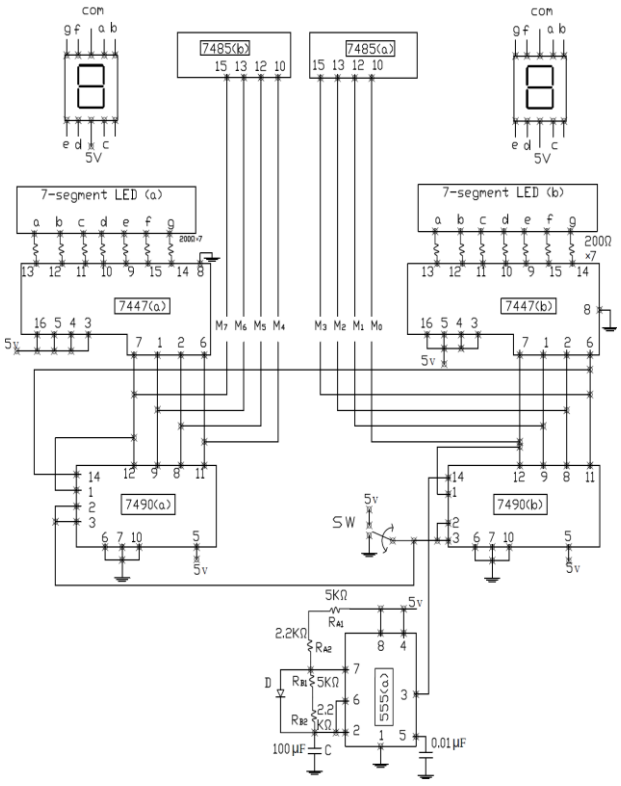


Fig.(3) The detailed wiring diagram of the chronometer by 555 oscillator

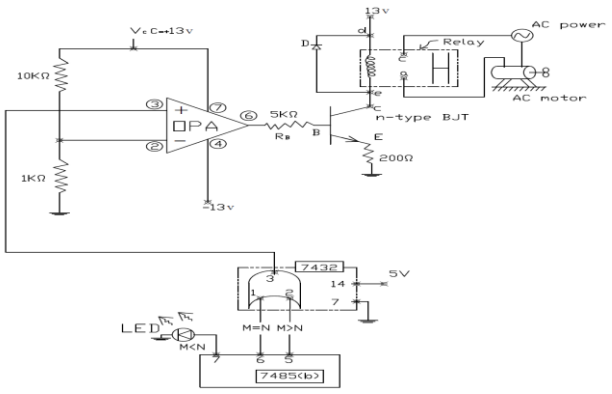


Fig.(5) The detailed diagram of the AC motor

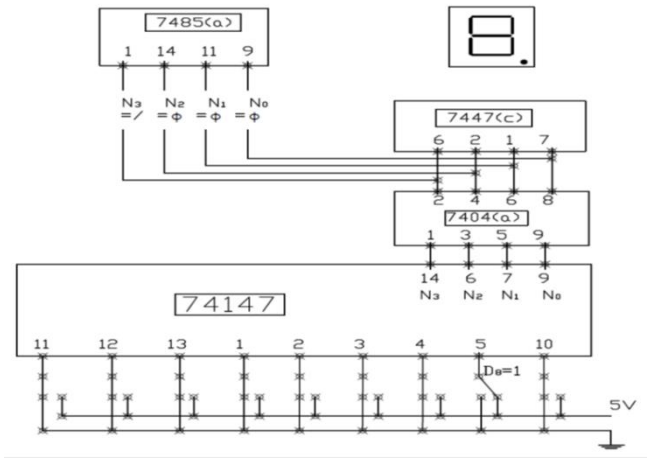


Fig.(6) The logic diagram of the encoder(10X3) when D_8=1 (t_s=8 sec)

IV. THE PRINCIPLE OF 555 ASTABLE MULTISTAGE OSCILLATOR

(1) In figure (7), the folding line represents the path that the 555 oscillator travels during the first charge. The folding line starts from point a and passes through b, d, e, and f points and finally flows to point g. Because the internal resistance R_d of the diode is about 5 Ω and much smaller than R_B = R_{B1} +R_{B2}=7.2KΩ, the current must pass through the abdefg route without passing through the R_B resistor. (the bf route and the bdef route are two parallel circuits. The current passing through is inversely proportional to the resistance.) At this time, the output voltage of the 555 oscillator (V_3=V_{out}) is the DC bias voltage V_{CC} (V_{out}= V_{CC} =V_3 = 5 V), which is represented by t_0.

(2) In figure (8), the folding line represents the route through which the 555 oscillator circulates during discharge. Because the diode is turned off due to the back-stop effect itself, the current cannot flow into the fedb segment. The route of the discharge current becomes g→f→b→7 (here, "7" refers to the 7th pin of the 555 oscillator).

(3) Calculate the time required (t_1) for discharging according to the resistance R_B passed through the discharge path (g→f→b→7) in figure (8).

t_1=R_B*C*ln2=(7.2X10^{3}Ω)*(100X10^{-6}F)*(ln2)=0.5(sec)

(4) Calculate the charging time (t_2) required after the second charging according to the charging path (a→ b→ d→ e→ f→ g) after the second charging in figure (9) (Because R_A =7.2KΩ>>R_D=5Ω, so R_D is ignored).

t_2=R_B*C*ln2=(7.2X10^{3}Ω)*(100X10^{-6}F)*(ln2)=0.5(sec)

(5) The output pulse of the oscillator after the second charge is shown as figure (10). If the unsteady state of the first charge is not counted, the period T is 1 second (T=1 sec) and the frequency f= 1/T=1/1=1 (Hz) of the remaining pulse waves.

(6) Connect the output pulse (digital pulse) of figure (10) to the 14th pin of logic IC7490(b) in figure(3)

as the input pulse of logic IC7490 (b) (negative-edge trigger pulse).

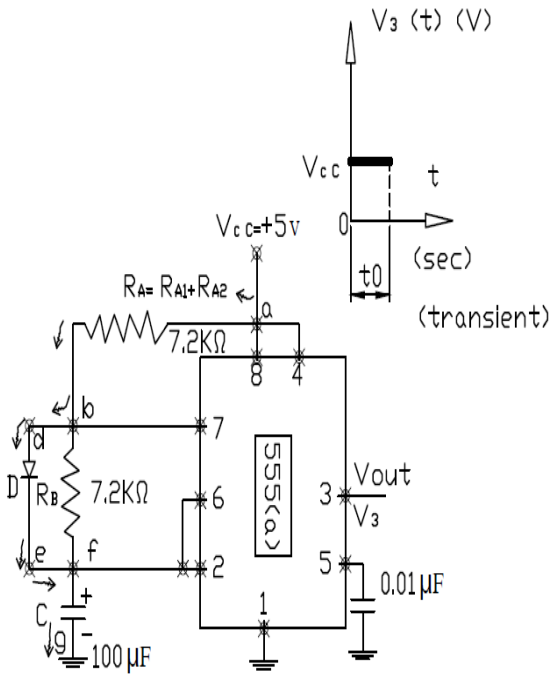


Fig.(7) The current path of the first charging

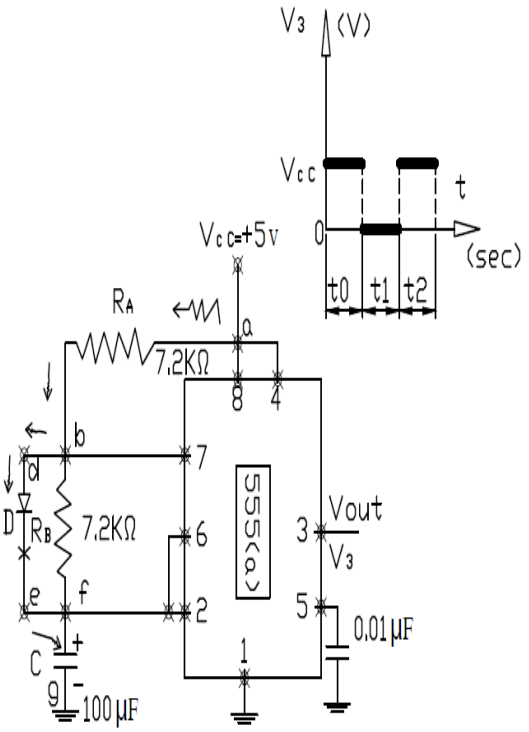


Fig.(9) The current path of the second charging

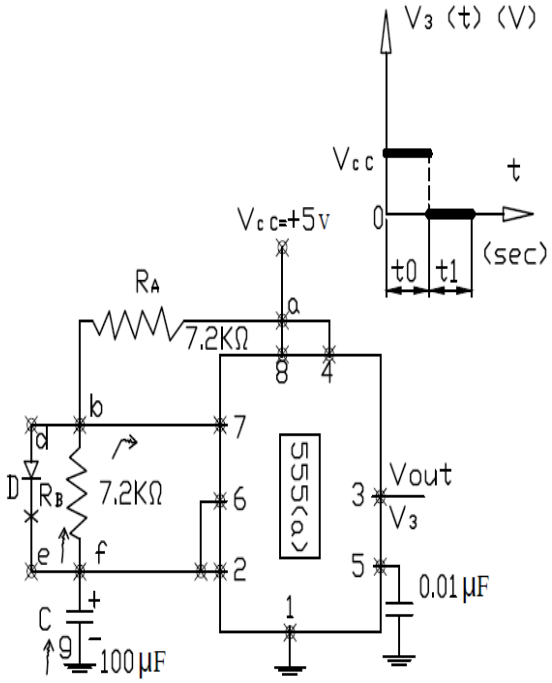


Fig.(8) The current path of the charging

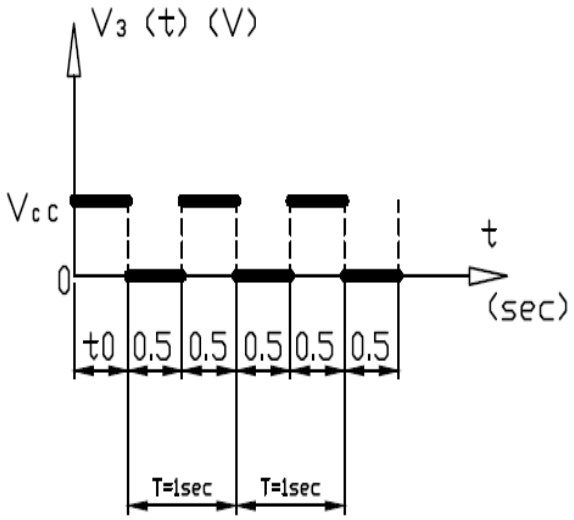


Fig.(10) The overall output pulse of 555 oscillator

V.THE PRINCIPLE OF MODULUS 100 UP COUNTER BY 555 OSCILLATOR

(1) When SW=/ (high potential), then, logic IC 7490(b) and 7490(a) are all cleared. The logic diagram is shown as figure (11). When SW=/ (high potential), this is the zeroing action of the chronometer. Although the digital pulse of the 555 oscillator continues to pass to CK (b), it still cannot excite IC7490(b). At this time, the display is 00.

(2) When SW=Ø (low potential), the logic state before the 40th trigger of CK(b) is shown as figure (12) and the display is 39.

(3) When SW=Ø (low potential), the first temporality after the 40th trigger of CK(b) is shown as figure (13). At this time, IC7490(b) returns to zero (ie, M_3:/→Ø and M_0:/→Ø). At the same time, the feedback of M_3:/→Ø causes CK(a):/→Ø (negative- edge trigger)

(4) When SW=Ø (low potential), the second temporality after the 40th trigger of CK (b) is shown as figure (14). The effect of CK(a):/→Ø (negative-edge trigger) causes IC7490(a) to enter a decimal number (ie, M_6:Ø→/, M_5:/→Ø, M_4:/→Ø)

(5) When SW=Ø (low potential), the third temporality after the 40th trigger of CK (b) is shown as figure (15) and the display is 40.

(6) When SW=Ø (low potential), the logic state before the 80th trigger of CK (b) is shown as figure (16) and the display is 79.

(7) When SW=Ø (low potential), the first temporality after the 80th trigger of CK(b) is shown as figure (17). At this time, IC7490(b) returns to zero (ie, M_3:/→Ø and M_0: /→Ø). At the same time, the feedback of M_3: /→Ø causes CK (a): /→Ø (negative-edge trigger) and the display is 70.

(8) When SW=Ø (low potential), the second temporality after the 80th trigger of CK(b) is shown as figure (18). At this time, CK(a):/→Ø (negative-edge trigger) causes the IC7490(a) to enter a decimal number (ie, M_7:Ø→/, M_6: /→Ø, M_5: /→Ø, M_4: /→Ø).

(9) When SW=Ø (low potential), the third temporality after the 80th trigger of CK(b) is shown as figure (19) and the display is 80.

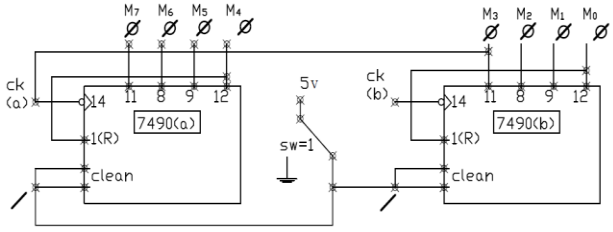


Fig.(11) The logic diagram for the case of SW=/ (5V)

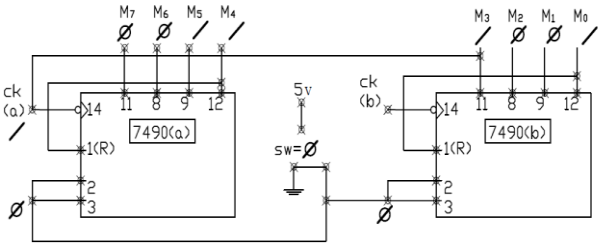


Fig.(12) The logic state before the 40th trigger at CK(b)

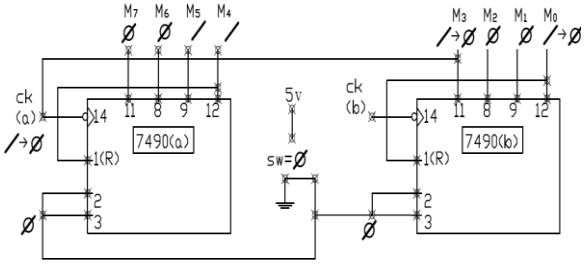


Fig.(13) The first temporality after the 40th trigger at CK(b)

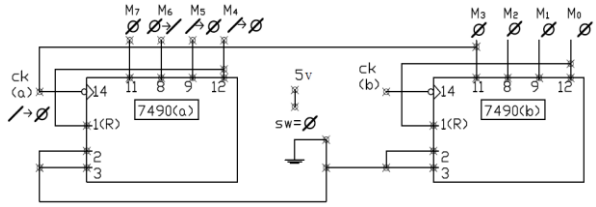


Fig.(14) The second temporality after the 40th trigger at CK(b)

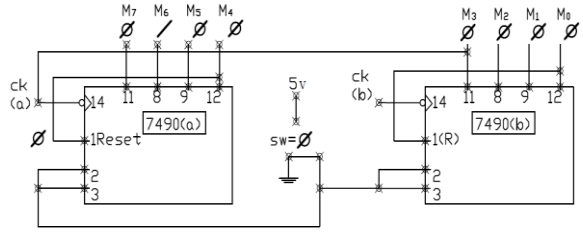


Fig.(15) The third temporality after the 40th trigger at CK(b)

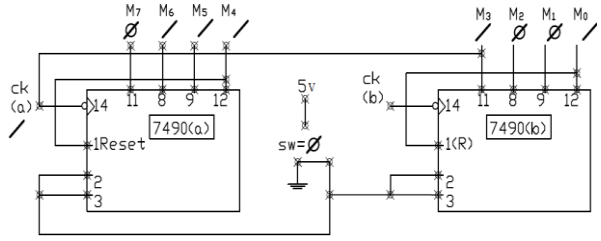


Fig.(16) The logic state before the 80th trigger at CK(b)

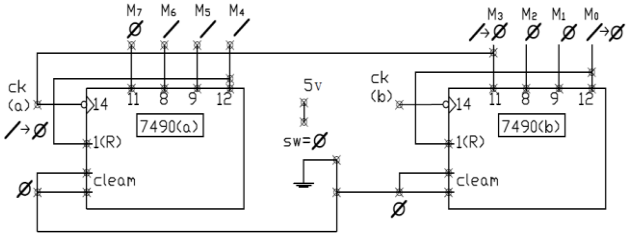


Fig.(17) The first temporality after the 80th trigger at CK(b)

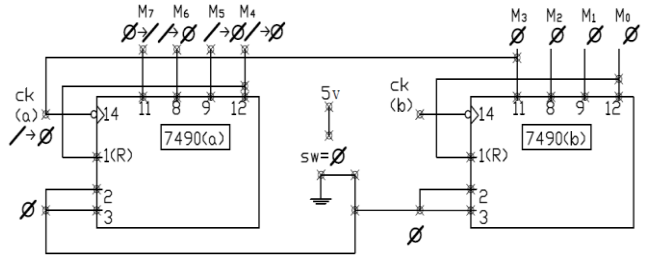


Fig.(18) The second temporality after the 80th trigger at CK(b)

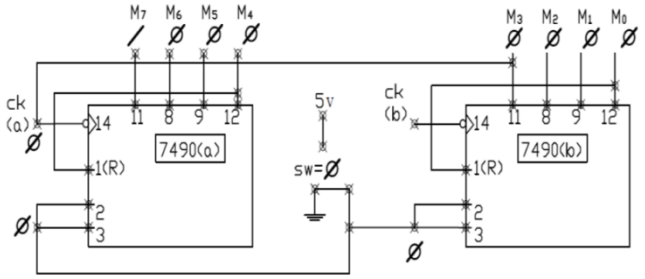


Fig.(19) The third temporality after the 80th trigger at CK(b)

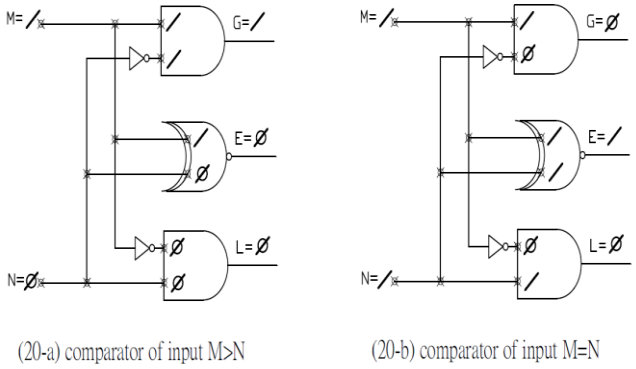
VI. THE PRINCIPLE OF 8-BIT MAGNITUDE COMPARATOR

(1) Figure (20) represents the logic diagram of a 1-bit magnitude comparator. When M>N is input, the output will be G=/ (greater), E=Ø (not equal), L=Ø (not lower) as shown in figure (20-a). When M =N is input, the output will be G= Ø (not greater), E=/ (equal), L =Ø (not lower) as shown in figure (20-b, c). When M<N is input, the output will be G =Ø (not greater), E=Ø (not equal), L=/ (lower) as shown in figure (20 -d).

(2) Figure (21~23) represent logic diagrams of 2-bit magnitude comparator composed of two 1-bit magnitude comparators. The meaning of case (1) is as follows. When the input is M>N, the output will be G=/ (greater), E=Ø (not equal), L=Ø (not lower) as shown in figure (21-a, b). The meaning of case (2) is as follows. When the input is M=N, the output will be G=Ø (not greater), E=/ (equal), L=Ø (not lower) as shown in figure (22-a, b). The meaning of case (3) is as follows. When the input is M<N, the output will be G=Ø (not greater), E=Ø (not equal), L=/ (lower) as shown in figure (23-a, b).

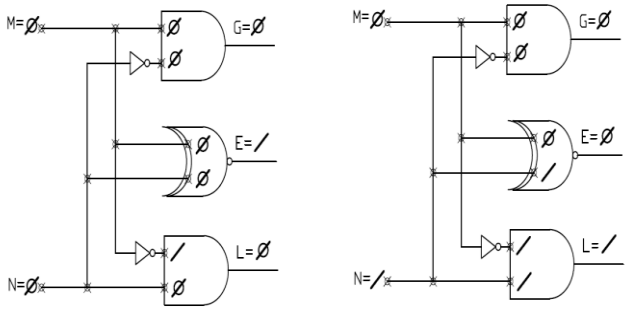
(3) Figure (24~26) represent logic diagrams of a 4-bit magnitude comparator composed of two 2-bit magnitude comparators. The meaning of case (1) is as follows. When the input is M>N, the output will be G=/ (greater), E=Ø (not equal), L=Ø (not lower) as shown in figure (24-a, b). The meaning of case (2) is as follows. When the input is M=N, the output will be G=Ø (not greater), E=/ (equal), L=Ø (not lower) as shown in figure (25-a, b). The meaning of case (3) is as follows. When the input is M<N, the output will be G=Ø (not greater), E=Ø (not equal), L=/ (lower) as shown in figure (26-a, b).

(4) Figure (27~29) represent logic diagrams of a 8-bit magnitude comparator composed of two 4-bit magnitude comparators. When the input is M>N, the output will be G=/ (greater), E=Ø (not equal), L=Ø (not lower), as shown in figure (27).When the input is M=N, the output will be G=Ø (not greater), E=/ (equal), L= Ø(not lower) as shown in figure (28). When the input is M<N, the output will be G=Ø (not greater), E=Ø (not equal), L=/ (lower) as shown in figure (29).



(20-a) comparator of input M>N

(20-b) comparator of input M=N



(20-c) comparator of input M=N

(20-d) comparator of input M<N

Fig.(20) 1-bit magnitude comparator

+

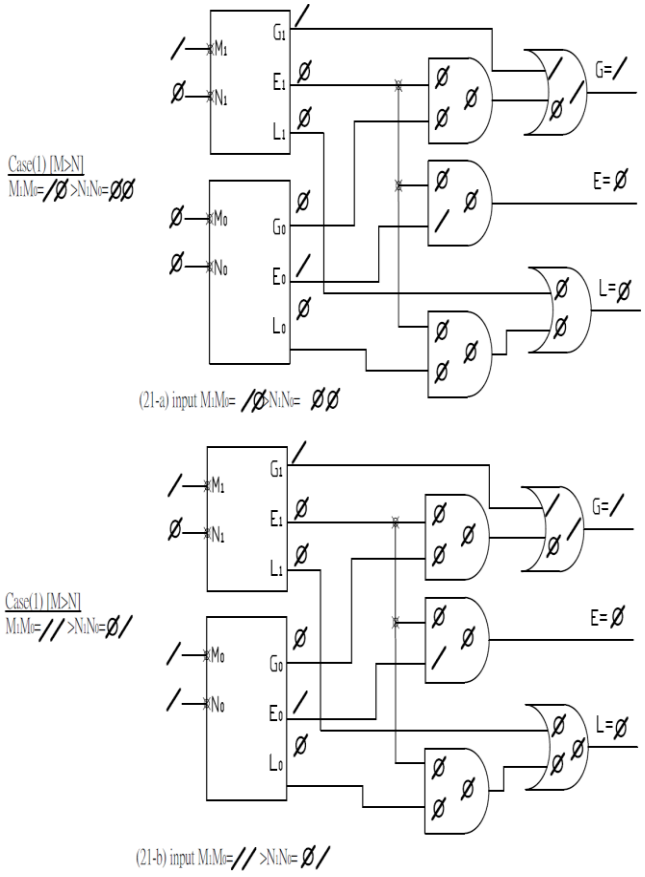
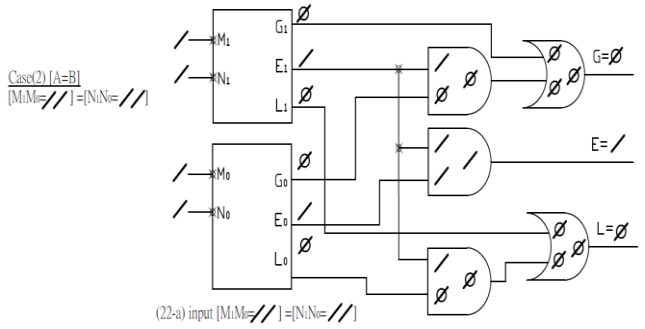


Fig.(21) 2-bit magnitude comparator when the input is M>N



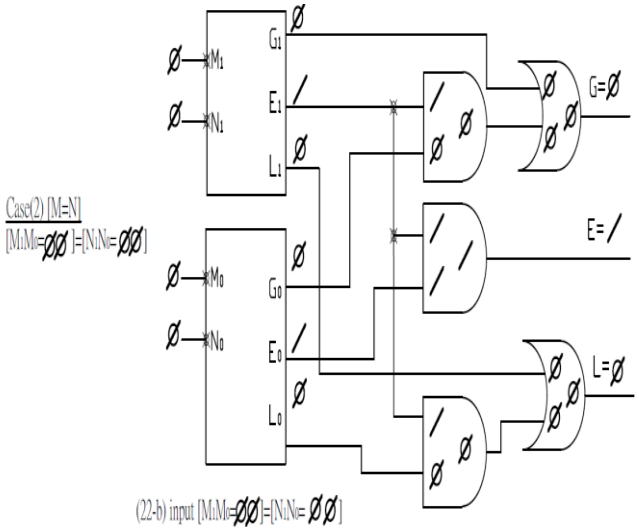


Fig.(22) 2-bit magnitude comparator when the input is M=N

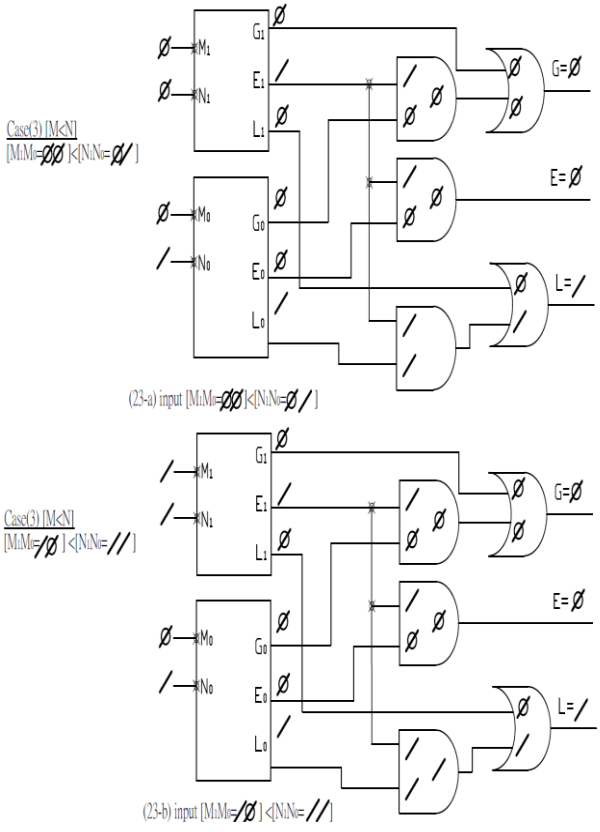
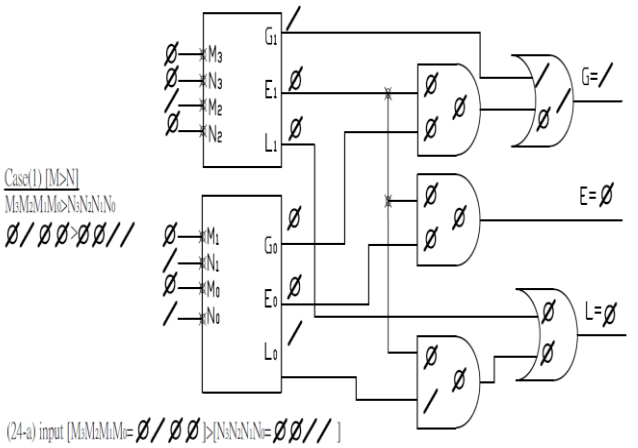


Fig.(23) 2-bit magnitude comparator when the input is M<N



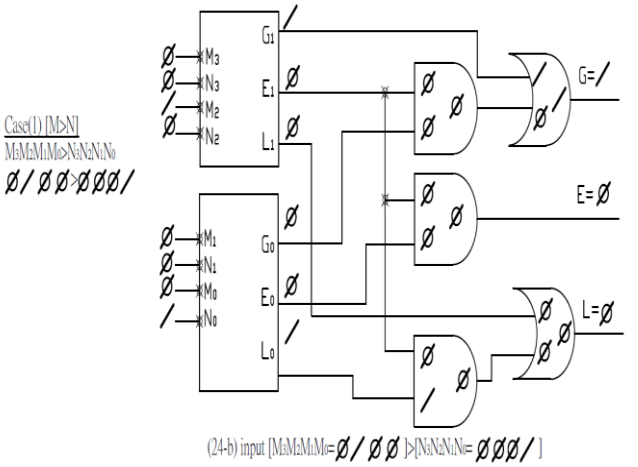
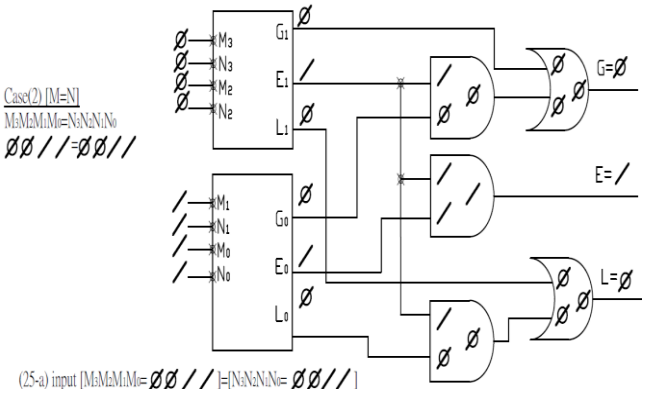


Fig.(24) 4-bit magnitude comparator when the input is M>N



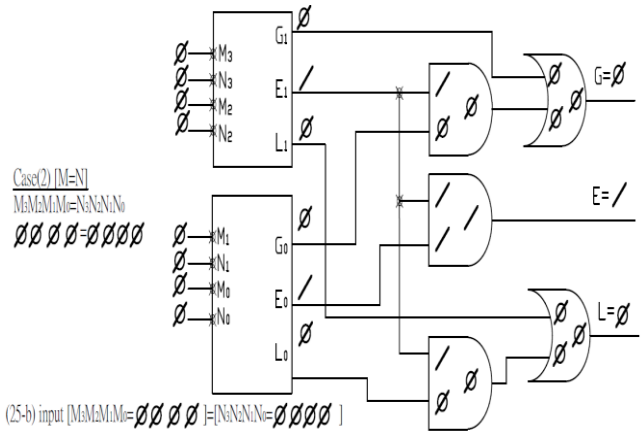
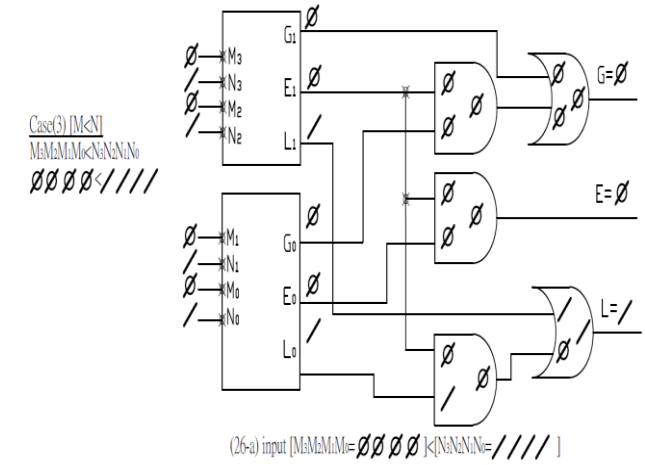


Fig.(25) 4-bit magnitude comparator when the input is M=N



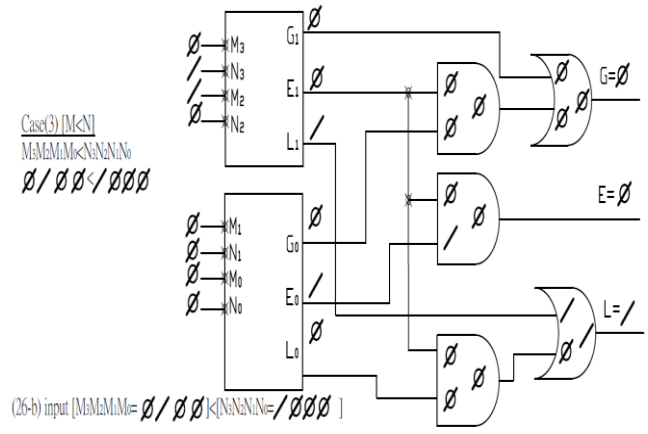


Fig.(26) 4-bit magnitude comparator when the input is M<N

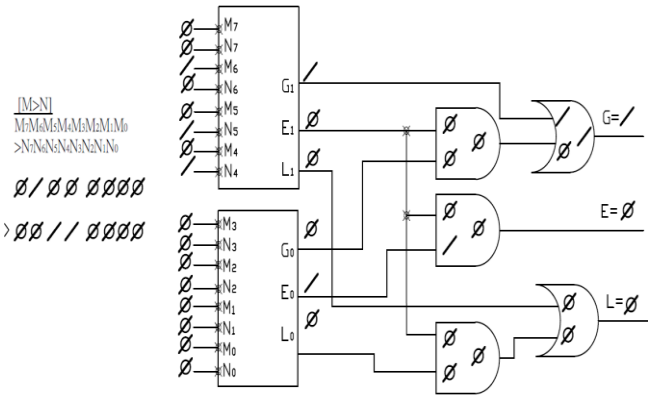


Fig.(27) 8-bit magnitude comparator when the input is M>N

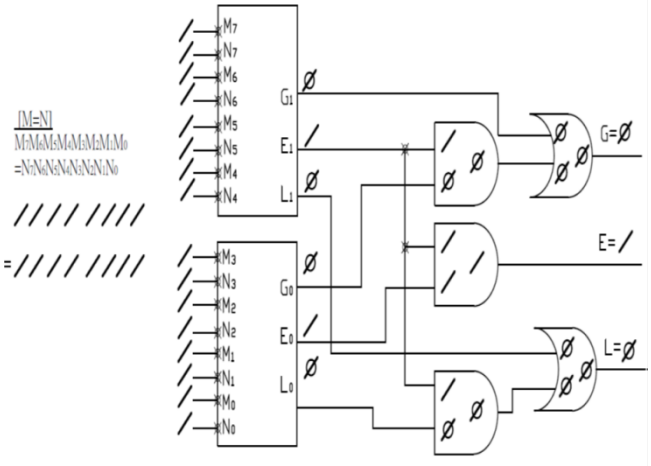


Fig.(28) 8-bit magnitude comparator when the input is M=N

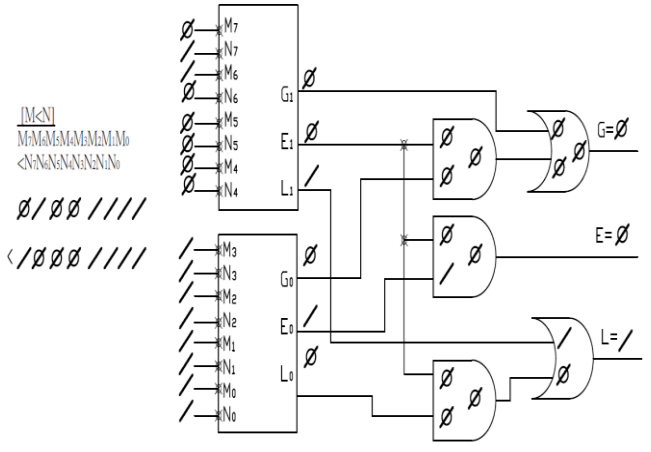


Fig.(29) 8-bit magnitude comparator when the input is M<N

VII. THE PRINCIPLE OF THE ALTERNATING CURRENT (AC) MOTOR

(1) When the input is $M_7M_6M_5M_4$ M_3 $M_2M_1M_0$<$N_7N_6N_5N_4N_3N_2N_1N_0$ (ie, M<N), the 7th pin output of IC7485 (b) is / (high potential) and the output of the 6th and 5th pins are Ø (low potential) shown as figure (30). This result will cause the LED to illuminate and the AC motor to stop as shown in figure (30).

(2) In figure (30), the 7th pin of IC7485 (b) is / (high potential, voltage is about 4.5V). Its connection with the LED can make the LED light. On the other side, the 5th and 6th pins of IC7485 (b) are both low potential Ø, which can make the positive terminal voltage V_+ of the operational amplifier approach zero. Calculate the negative terminal voltage V_- of the operational amplifier according to the voltage division rule as shown below.

$$V_-=13V*\frac{1K\Omega}{(10+1)K\Omega}=1.18V \quad ---①$$

According to the comparison function of the operational amplifier, the output voltage is V_6 (V_{out})=-13V because (V_+=0V)< (V_-=1.18V).

(3) The base current I_B of the BJT becomes outflow (ie, flow from point B to point 6) causing the BJT transistor to turn off as shown in figure (30). At the same time, the relay is off (ie, normally open) and the AC current is interruption and the AC motor is stopped.

(4) When the input is $M_7M_6M_5M_4M_3$

$M_2M_1M_0=N_7N_6N_5N_4N_3N_2N_1N_0$ (ie, M=N), the 6th pin output of IC7485 (b) is / (high potential) and the output of the 7th and the 5th pins are Ø (low potential) shown as figure (31). This result will cause the AC motor to operate and cause the LED to go out as shown in figure (31).

(5) In figure (31), the 7th pin of IC7485 (b) is Ø (low potential, the voltage is about 0V). Its connection with the LED can make the LED off. On the other side, the 6th pin of IC7485 (b) is / (high potential) and the 5th pin of IC7485 (b) is Ø (low potential). The 5th and the 6th pins are simultaneously entered the OR gate and the output is / (high potential). Because the positive terminal voltage of the operational amplifier (V_+=4.5V) is greater than the negative terminal voltage (V_-=1.18 V) [V_+>V_-], the output voltage is a positive DC bias voltage ($V_6=V_{out}=+V_{CC}$=+13V).

(6) In figure (31), it is assumed that the BJT transistor operates in the saturation region, the threshold voltage V_{BE}=0.8V between the base B and the emitter E, and the threshold voltage V_{CE}=0.2V between the collector C and the emitter E. Calculate the voltage along the loop 6→B →E →g. According to Kirchhoff's voltage law:

$V_B-I_BR_B-V_{BE}=0 \rightarrow 13-I_B*5-0.8=0$

$\rightarrow I_B=2.44(mA)$ ----------②

(7) In figure (31), calculate the voltage along the loop: d →e →C →E →g that is according to Kirchhoff's voltage law.

$V_{CC}-I_C*1K\Omega-V_{CE}=0 \rightarrow 13-I_C*1-0.2=0 \rightarrow I_C=12.8(mA)$ ----------③

In the above calculation process, 1KΩ is the approximate value and that is representing the impedance of the induction coil in the relay.

(8) Because (I_C=12.8mA) < (ßI_C= 150x 2.44 =366mA), it can be confirmed that the BJT transistor operates in the saturation region, which means that V_{BE}=0.8V is correct before.

(9) On the internal path of the relay, since the induction coil generates magnetism to attract the H-type cast iron (b) to the ca terminal, the ca terminal can pass current. Because the ca terminal can pass current, the AC power supply can completely enter the motor to make the motor run. A diode is connected to the outer end of the relay to protect the coil of the relay from reverse flow of the I_C current.

(10) When the inpu$M_7M_6M_5M_4M_3M_2M_1M_0$>$N_7N_6N_5N_4N_3N_2N_1N_0$ (ie, M>N), the 5th pin output of IC7485 (b) is / (high potential) and the output of the 7th and the 6th pins are Ø (low potential) shown as figure (32). This result will cause the AC motor to operate and cause the LED to go out as shown in figure (32).

(11)In figure (32), the 7th pin of IC 7485 (b) is Ø (low potential, the voltage is about 0V). Its connection with the LED can make the LED off. On the other side, the 6th pin of IC7485 (b) is Ø (low potential) and the 5th pin of IC7485 (b) is / (high potential). The 5th and 6th pins are simultaneously entered the OR gate and the output is / (high potential). Subsequent operational amplifier, npn-type BJT transistor, relay, and AC motor operate in exactly the same way as item (5)(6)(7)(8)(9), so they are not explained again.

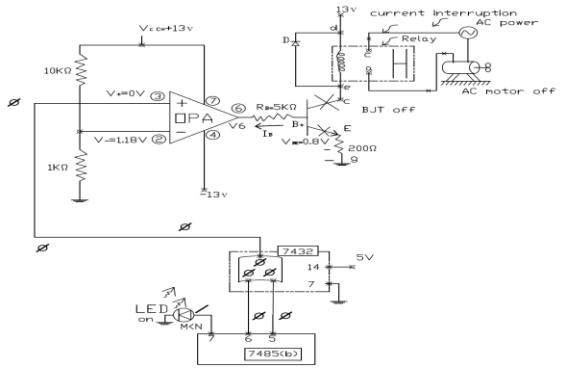


Fig.(30) The detailed current diagram of AC motor in the case of M<N

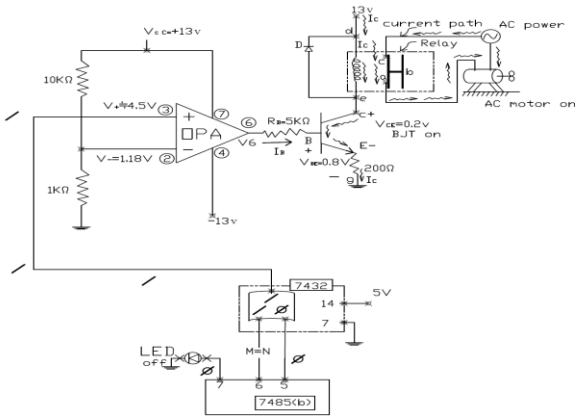


Fig.(31) The detailed current diagram of AC motor in the case of M=N

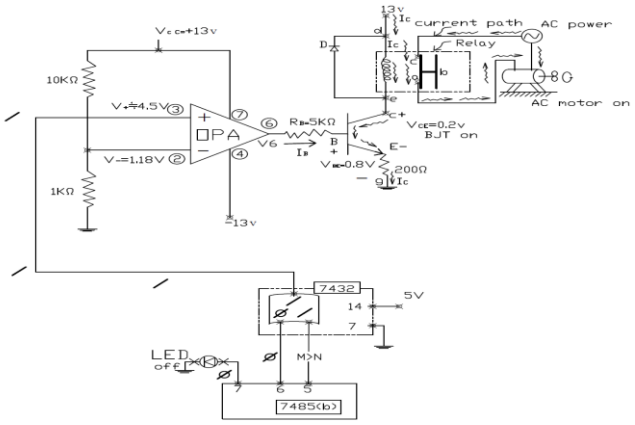


Fig.(32) The detailed current diagram of AC motor in the case of M>N

VIII. COMPLETED PHOTO.

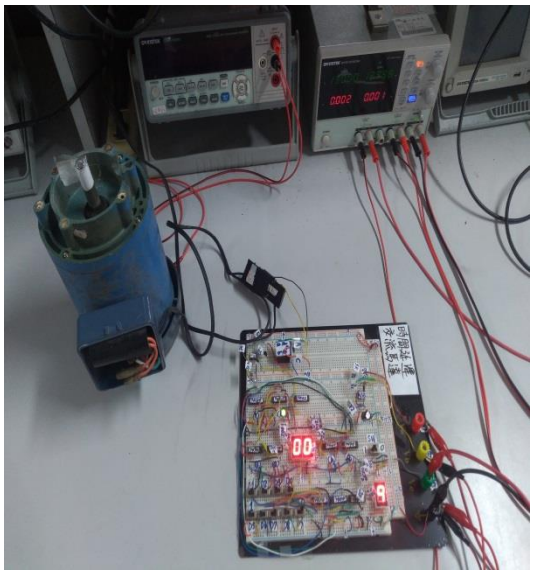


Fig.(33) completed photo.

IX. EXPERIMENT DATA (THE TRUTH TABLE)

Table 1

Selection button	7-segment LED display(c)(delay seconds t_s(sec))	The number of seconds that the motor is delayed
D_1=/	1	1
D_2=/	2	2
D_3=/	3	3
D_4=/	4	5
D_5=/	5	5
D_6=/	6	6
D_7=/	7	7
D_8=/	8	8
D_9=/	9	9

X.CONCLUSION

(1) In figure (31) and (32), a 200Ω resister is placed between the emitter (E) and ground (g) of the BJT transistor. This resister acts as a current limiting resister. This current limiting resistor is to make the operation of the BJT transistor more stable. When the currents of I_C and I_B are calculated by the Kirchhoff's voltage law in the calculation of the AC motor system in the previous item VII, the influence of the 200Ω resistor is not counted.

(2) The output of pin 6 of IC7485 (b) is / (high potential) because the input is M=N in figure (31). The output of pin 5 of IC7485 (b) is / (high potential) because the input is M>N in figure (32). Because the 5th and 6th pin of IC7485 (b) are transferred to OR gate, then M=N and M>N will make the output of IC7432 is / (high potential) and have the same analog current flow and AC motor start.

(3) The main reason why the motor of this paper is only suitable for AC motor and not suitable for DC motor is that the voltage source V_{CC}=5V of DC motor is the same as the DC voltage source of logic IC7490. If a DC motor is used, the vibration of the DC motor will affect the stability of the voltage source V_{CC} and interfere with the order of the sequential logic IC7490. This will destroy the function of the timer.

(4) In figure (7), t_0 time is the time required for the first charge of the 555 oscillator. Because the calculation of the t_0 time is very complicated, so it is not calculated in detail in this paper.

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