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Calculation of Power Losses of MOSFET Transistors by Experimental Data

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***Abstract*—A methodology for the calculation of power losses of MOSFET transistors working in switch mode power supply converters is presented in this article. The calculation is based on experimental results (time-diagrams) for the drain current and drain-source voltage of the transistors. There is an analysis of the work of the MOSFET transistor using the experimental graphs of drain current and of drain-source voltage. The graphs of drain current and drain-source voltage are found out as a composed of linear sections. There are worked out equations and are obtained expressions to determine the power losses of MFSFET transistors There is presented also the sequence of operations for calculating the power losses of semiconductor devices by experimentally obtained drain current and drain-source voltage graphs. This methodology is applicable under conditions defined in this article.**

Keywords—switch mode power supply; power converter; MOSFET losses; power losses; PWM

I. INTRODUCTION

The determination of power losses in MOSFET transistors of switch mode power supply (SMPS) converters is an essential moment during the design and working-up of power electronic devices. Some authors [1-6] propound the determination of power losses in MOSFET transistors of SMPS converters to be done on the basis of catalogue data: drain-source on-state resistance, $R_{DS(ON)}$; parasitic capacitances C_{gs}, C_{gd} and C_{ds}. In [8] is suggested a method for determination of conduction and commutation losses in MOSFET transistors using a catalogue information of manufactures. The use of the method suggested by the authors is applicable when the current form is close to rectangular and trapezoid, and possibility of determination either the current through the transistor or the current through the anti-parallel diode from its structure is available.

There is shown an idealized form of current I_D and voltage drop U_{DS} upon power transistors in SMPS converters in Fig. 1. The time interval t_{ON} is the duration of switch on condition (ON transistor), while t_{OFF} is the pause duration between impulses (OFF transistor), and T_{SW} is the period of impulses' repeating.

The realibility and exploration time of powerful MOSFET transistor are in direct dependence on crystal temperature, which is depending on the power dissipated on it.

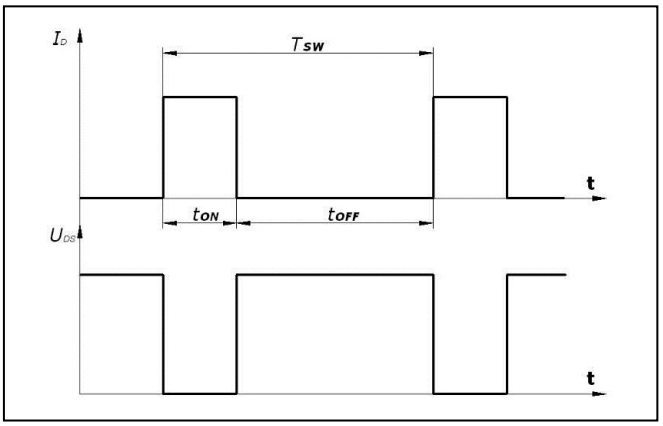

Fig. 1. *Time-dependence of drain current, I_D, and drain-source voltage, U_{DS}, of MOSFET transistor in switch mode regime.*

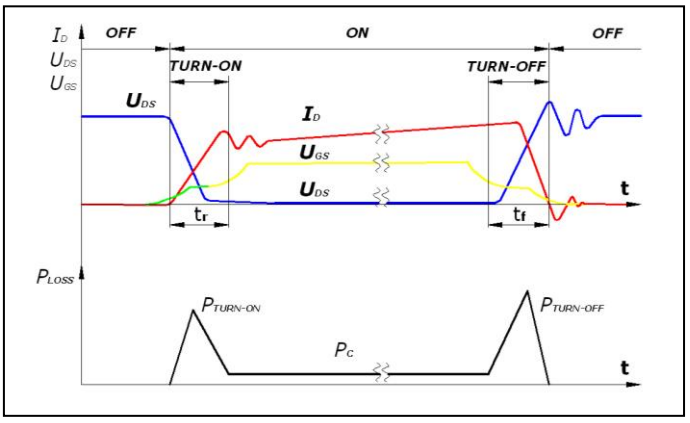

Fig. 2. *Time-dependence of drain current, drain-source voltage and power losses of MOSFET transistor during switch mode regime.*

The power losses received during the operation of MOSFET transistors in switch mode regime are static and dynamic (Fig. 2), and they can be divided in three groups according to [8]:

- Conduction losses, P_C, are the losses in ON transistor depending on the drain current and the parameters of the ON transistor (drain source on-state resistance, $R_{DS(ON)}$);
- Commutation losses, P_{SW}. These are the dynamic losses arising during the transition process of

turn-on, $P_{TURN-ON}$, and of turn-off, $P_{TURN-OFF}$, of the transistor. $P_{SW} = P_{TURN-ON} + P_{TURN-OFF}$

- Leak losses, P_b. These are the losses during the time of OFF transistor. In this case, the drain current has a small value (of the order of μA [9]) that is why the losses are insignificant and we can neglect them

- For the losses in MOSFET transistor the following expression [8] can be written down:

$$P_{LOSS} = P_C + P_{SW} + P_b \approx P_C + P_{SW} \quad (1)$$

The purpose of this study is to propose a methodology for calculation of power losses in MOSFET transistors used in SMSP converters on the ground of data from experimentally obtained time-diagrams of current through transistors and drain-source voltage upon them.

II. AN ANALYSIS OF POWER TRANSISTORS LOADING

It is used a scheme of full-bridge DC-DC converter to analyse and calculate the power losses in MOSFET transistors.

The basic scheme of the converter is represented in Fig. 3 [10,11]. The convertor consists of: transistors VT1, VT2, VT3, and VT4; diodes D1, D2, D3, and D4 included in anti-parallel in their structure; isolating step-down transformer VTr1; rectifiers VD5 and VD6; output filter inductor L1, and filter capacitor C2.

The operation of the converter is examined in details and analyzed on the basis of time-diagrams (oscillograms) for the current and voltage drop upon the elements which are obtained though simulated examination [12,13].

The power transistors' loading is analysed through a simulated examination carried out by the simulator *Cadence PSpice*.

There is a presentation of the results of simulated examination regarding operation of transistor in Fig. 4, Fig. 5, and Fig. 6. The controlling impulses (UgsVT1 and UgsVT3, UgsVT2 and UgsVT4) of transistors VT1 and VT3, VT2 and VT4; the current through transistor I_D and the drain-source voltage U_{DS} are presented in Fig. 4. There are illustrated the current through transistor, I_D, and the drain-source voltage, U_{DS}, during the transition process of turn-on and turn-off of transistor in Fig. 5 and Fig. 6. The peculiar time moments $t_0, t_1, t_2, t_3, t_4, t_5$, and t_6 of transistor's operation are marked in Fig. 4.

The time interval from the moment t_0 to t_6 corresponds to the period of impulses T_{SW}. The operation of transistor VT4 during the time intervals indicated in Fig. 4 possesses the following peculiarities:

- The time interval t_0 - t_1 characterizes the transition process of turn-on of the anti-parallel connected diode from the structure of transistor VT4;
- The time interval $t_1 – t_2$ is the interval when the anti-parallel connected diode is on;
- During the time interval $t_2 – t_3$ a transfer of the current from the diode upon the transistor is done at the moment t_2 at current $I_D=0$ and drain-source voltage, $U_{DS}=0$. In this interval MOSFET transistor VT4 is on, as the current increases from 0 to its maximum magnitude;
- In the time interval $t_3 – t_4$ the transistor VT4 remains on to assure running of self-induction current of transformers' primary winding during the pause. The drain current I_D decreases exponentially. The drain current I_D and drain-source voltage U_{DS} can be approximated to linear form for the needs of engineering calculations;
- The time interval $t_4 – t_5$ is a transition process of transistor VT4 turn-off, which is illustrated in Fig. 6. The current decreases up to zero, and the supply voltage is put on the drain-source junction of the transistor;
- During the time interval $t_5 – t_6$ the transistor VT4 is off, the current through it is zero, and the supply voltage put on the drain-source junction of the transistor.

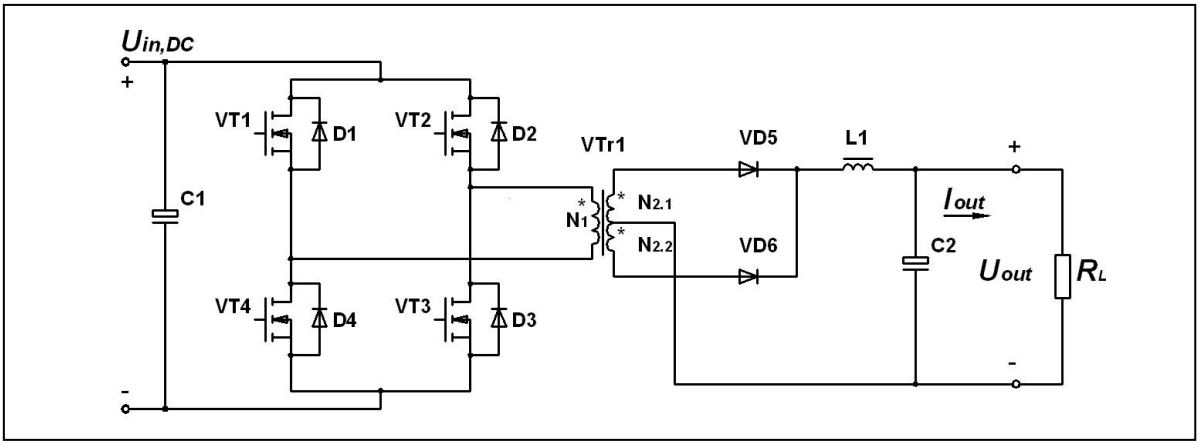

Fig. 3. *A basic scheme of full-bridge DC-DC converter*

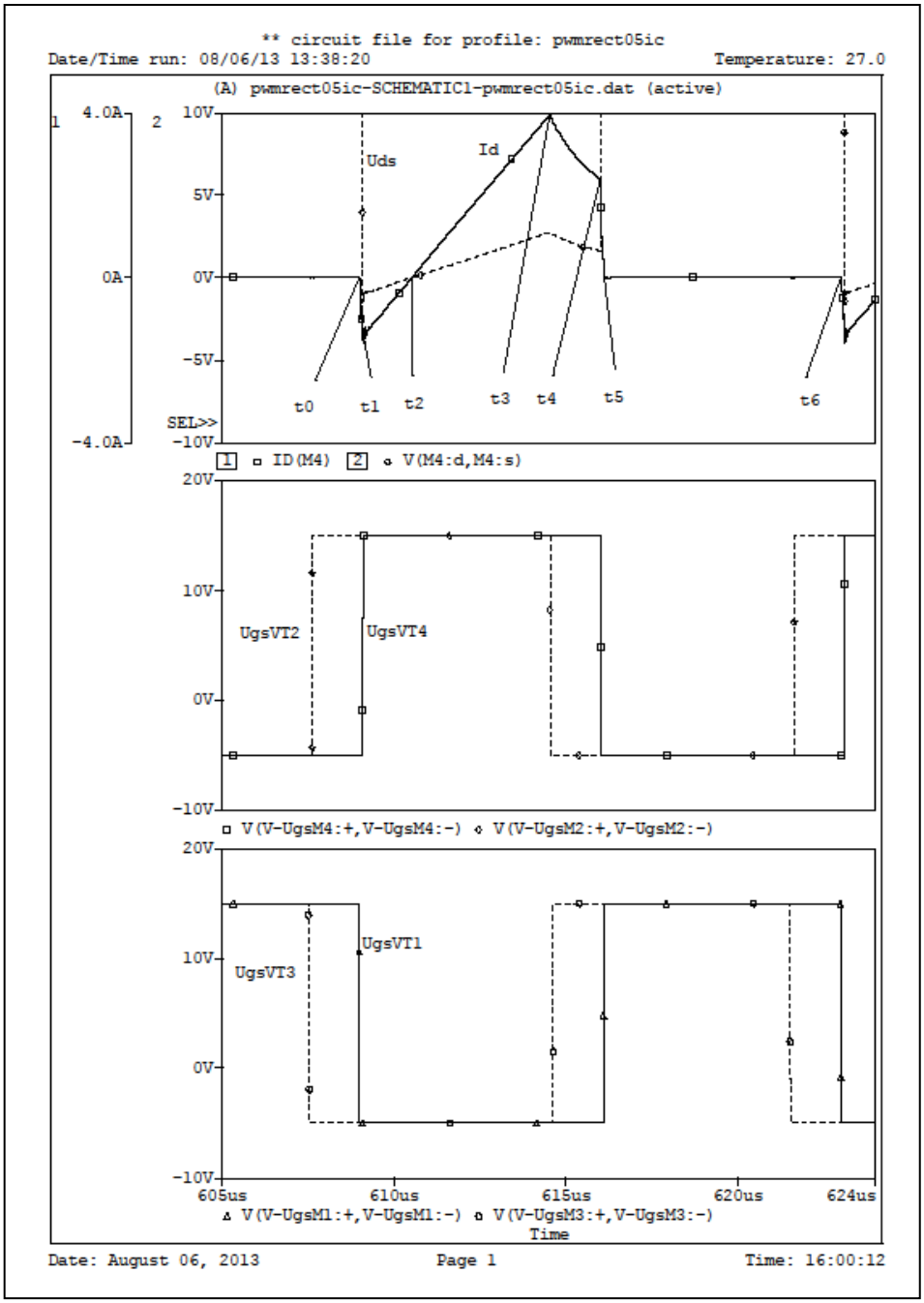

Fig. 4. *Time-diagrams of the operation of transistor VT4 for one period*

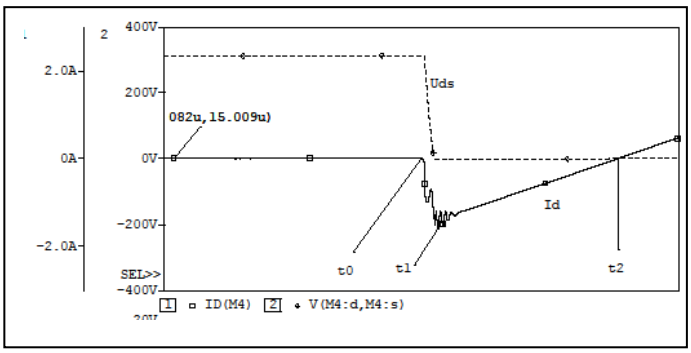

Fig. 5. *Time-diagram for the operation of transistor VT4 at turn-on.*

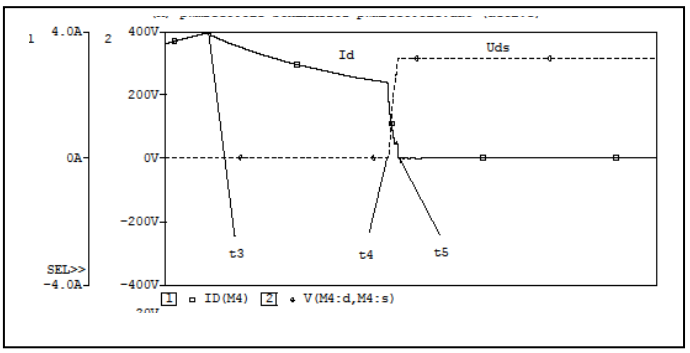

Fig. 6. *Time-diagram for the operation of transistor VT4 at turn-off.*

The analysis of the represented in Fig. 4, Fig. 5, and Fig. 6 time-diagrams shows that:

- The current through the transistor and through anti-parallel connected diode from the its structure cannot be measured separately;
- When the transistor is switch on both the current and the voltage drop upon the transistor change to a relatively wide range.
- The oscillograms obtained from the simulated examination give an opportunity for precise calculation of transistor's power losses.

It is necessary to take into account the fact that during elaboration of electronic devices the simulation of their functioning is an essential stage of a design. By that reason, the proposal is to develop methodology of MOSFET transistor power losses' calculation using the results obtained by the simulated examination of the shown scheme.

III. A METHODOLOGY FOR CALCULATION OF MOSFET TRANSISTORS POWER LOSSES

The methodology for determination of power losses by data from the experimental results is based on time-diagrams of MOSFET transistor's VT4 functioning. The presentation of these diagrams is in Fig. 4, Fig. 5, and Fig. 6.

The dissipation of the power upon the MOSFET transistor in any time moment is equal to the product of the current and the voltage on it:

$$p_{LOSS}(t) = u_{DS}(t) \cdot i_D(t) \quad (2)$$

Where:

$u_{DS}(t)$ is the moment value of the drain-source voltage of transistor;

$i_D(t)$ is the moment value of drain current through the transistor.

Integrating the equation written above for the period T_{SW}, we get the transistor power losses as:

$$P_{LOSS} = \frac{1}{T_{SW}} \int_0^{T_{SW}} p_{LOSS}(t) \cdot dt =$$

$$= \frac{1}{T_{SW}} \int_0^{T_{SW}} u_{DS}(t) \cdot i_D(t) \cdot dt \quad (3)$$

In accordance with the time intervals presented in Fig. 4, Fig. 5, and Fig. 6 and applying an integration of each interval the transistor's power losses are as follows:

$$P_{LOSS} = \frac{1}{T_{SW}} \sum_{j=1}^{k} \int_{t_{j-1}}^{t_j} u_{DS_j}(t) \cdot i_{D_j}(t) \cdot dt \quad (4)$$

Where:

$i_{D_j}(t)$ is the moment value of the drain current through the transistor during j^{-th} interval;

$u_{DS_j}(t)$ is the moment value of the drain-source voltage during j^{-th} interval;

k is the number of the intervals.

It is necessary to be determined the analytical form of the integral function for the solution of integrals. The analysis of time-diagrams presented in Fig. 4, Fig. 5, and Fig. 6 shows that the drain-source voltage, $u_{DS_j}(t)$, for the corresponding time interval is a linear function, passing across the points $(t_{j-1}, U_{DS_{j-1}})$ and (t_j, U_{DS_j}). For equation of the integral function, we get:

$$\frac{t - t_{j-1}}{t_j - t_{j-1}} = \frac{u_{DS_j}(t) - U_{DS_{j-1}}}{U_{DS_j} - U_{DS_{j-1}}} \quad (5)$$

Where:

$U_{DS_{j-1}}$ is the drain-source voltage at the moment t_{j-1};

U_{DS_j} is the drain-source voltage at the moment t_j.

After the transformation of (5) we get the following expression for the drain-source voltage in j^{-th} interval:

$$u_{DS_j}(t) = \frac{U_{DS_j} - U_{DS_{j-1}}}{t_j - t_{j-1}}(t - t_{j-1}) + U_{DS_{j-1}} \quad (6)$$

Let: $$K_{U_j} = \frac{U_{DS_j} - U_{DS_{j-1}}}{t_j - t_{j-1}}$$

After the substitution of the above expression in (6), we get:

$$u_{DS_j}(t) = K_{U_j} \cdot (t - t_{j-1}) + U_{DS_{j-1}} \quad (7)$$

By analogy for the linear function of current, $i_{D_j}(t)$, passing across the points $(t_{j-1}, I_{D_{j-1}})$ and (t_j, I_{D_j}) we get the following expression:

$$\frac{t - t_{j-1}}{t_j - t_{j-1}} = \frac{i_{D_j}(t) - I_{D_{j-1}}}{I_{D_j} - I_{D_{j-1}}} \quad (8)$$

Where:

$I_{D_{j-1}}$ is the drain current at the moment t_{j-1};

I_{D_j} is the drain current at the moment t_j.

After the transformation of (8) we get for the moment value of current through the transistor as follows:

$$i_{D_j}(t) = \frac{I_{D_j} - I_{D_{j-1}}}{t_j - t_{j-1}}\left(t - t_{j-1}\right) + I_{D_{j-1}} \quad (9)$$

Let: $$K_{I_j} = \frac{I_{D_j} - I_{D_{j-1}}}{t_j - t_{j-1}}$$

After that, the expression for the drain current acquires the following form:

$$i_{D_j}(t) = K_{I_j} \cdot \left(t - t_{j-1}\right) + I_{D_{j-1}} \quad (10)$$

Replacing in (2) the obtained expressions for the drain-source voltage (7) and drain current (10), we get the following expression for the moment value of power losses in transistor for the j^{-th} interval:

$$p_{LOSS_j}(t) = K_{U_j} \cdot K_{I_j} \cdot \left(t - t_{j-1}\right)^2 + \\ + \left(K_{U_j} \cdot I_{D_{j-1}} + U_{DS_{j-1}} \cdot K_{I_j}\right) \cdot \left(t - t_{j-1}\right) + \\ + U_{DS_{j-1}} \cdot I_{D_{j-1}} \quad (11)$$

Let:

$$A_j = K_{U_j} \cdot K_{I_j} = \\ = \frac{U_{DS_j} - U_{DS_{j-1}}}{t_j - t_{j-1}} \cdot \frac{I_{D_j} - I_{D_{j-1}}}{t_j - t_{j-1}} \quad (12)$$

$$B_j = K_{U_j} \cdot I_{D_{j-1}} + U_{DS_{j-1}} \cdot K_{I_j} = \\ = \frac{U_{DS_j} - U_{DS_{j-1}}}{t_j - t_{j-1}} \cdot I_{D_{j-1}} + U_{DS_{j-1}} \cdot \frac{I_{D_j} - I_{D_{j-1}}}{t_j - t_{j-1}} \quad (13)$$

$$C_j = U_{DS_{j-1}} \cdot I_{D_{j-1}} \quad (14)$$

After the replacement of (12), (13) and (14) in (11) we get the following expression for the moment values of power losses for j^{-th} interval:

$$p_{LOSS_j}(t) = A_j \cdot \left(t - t_{j-1}\right)^2 + \\ + B_j \cdot \left(t - t_{j-1}\right) + C_j \quad (15)$$

After integration of (15) the expression for the power losses for j^{-th} interval is:

$$P_{LOSS_j} = \frac{1}{T_{SW}} \int_{t_{j-1}}^{t_j} \left(A_j \cdot \left(t - t_{j-1}\right)^2 + B_j \cdot \left(t - t_{j-1}\right) + C_j\right) \cdot dt = \\ = \frac{1}{T_{SW}} \left[A_j \frac{\left(t_j - t_{j-1}\right)^3}{3} + B_j \frac{\left(t_j - t_{j-1}\right)^2}{2} + C_j \cdot \left(t_j - t_{j-1}\right) \right] \quad (16)$$

After replacing A_j, B_j, and C_j with the correspondent expressions in (16), we get the following equation for the power losses for the j^{-th} interval:

$$P_{LOSS_j} = \frac{1}{T_{SW}} \cdot \left\{ \left(U_{DS_j} - U_{DS_{j-1}}\right) \cdot \left(I_{D_j} - I_{D_{j-1}}\right) \cdot \frac{\left(t_j - t_{j-1}\right)}{3} + \right. \\ + \left[\left(U_{DS_j} - U_{DS_{j-1}}\right) \cdot I_{D_{j-1}} + U_{DS_{j-1}} \cdot \left(I_{D_j} - I_{D_{j-1}}\right) \right] \cdot \frac{\left(t_j - t_{j-1}\right)}{2} + \\ \left. + U_{DS_{j-1}} \cdot I_{D_{j-1}} \cdot \left(t_j - t_{j-1}\right) \right\} \quad (17)$$

As a result, for the power losses of MOSFET transistor we get the following expression:

$$P_{LOSS} = \sum_{j=1}^{k} \frac{1}{T_{SW}} \int_{t_{j-1}}^{t_j} u_{DS_j}(t) \cdot i_{D_j}(t) \cdot dt =$$

$$= \left(P_{LOSS_1} + P_{LOSS_2} + ... + P_{LOSS_k} \right) \quad (18)$$

The power losses of MOSFET transistors are determined in the following sequence:

1) The oscillogram of drain current I_D and drain-source voltage U_{DS} of transistor is registered in suitable scale.
2) The characteristic time points (t_0, t_1, t_2, t_3, … t_k) of the transistor's functioning are determined from the oscillogram. These time moments are defined at the points of changing the rate of increase and decrease of drain current I_D, and of drain-source voltage U_{DS} (these are the points where graph's gradient changes).
3) The values of the drain current I_D and of the drain-source voltage U_{DS} are read for any particular time point from the graph.
4) A calculation of power losses.

   The power losses are calculated for each time interval (t_j , t_{j-1}) according to (17).

The transistor's power losses are equal to the sum of those ones of each particular time intervals. The calculation is with accordance to (18).

IV. Conclusion

A methodology for the calculation of power losses of MOSFET transistors used in switch mode power supply converters is proposed. To implement that methodology a necessary condition is that the graphs of current through the transistor and of the drain-source voltage have to change in a linear form, or there is a possibility for these graphs to approximate to a linear function. The methodology may also serve for calculating the power losses of IGBT transistors and diodes.

The calculations of power losses can be accomplished either by time-diagrams received from simulated examinations or by oscillograms recorded from real electric scheme.

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