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# A Capacitor-Less CMOS Adaptively Biased Low-Dropout Regulator with Buffer for Portable On-Chip Application

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***Abstract*—This paper presents a capacitor-less low-dropout regulator (LDR), with adaptive bias (AB) and buffer structure for power management. Adaptive bias structure consists of current mirrors, which increase sensitivity for change of load current with low dissipation of small quiescent current, and make LDR more accurate. Buffer structure also consists of current mirrors and triode. By using the buffer, the stability of the LDR has been increased and the phase margin is over 54° with full range of load current from 100uA to 100mA. At maximum load current, the LDR's current efficiency is 99.50% with 1.8V power supply and 1.5V output. The power-supply rejection ration at 1 kHz is 77.64dB with 1mA and -48.52dB with 100mA load current. The LDR Performance of the proposed LDR is verified with 0.11-um COMS process.**

***Keywords — low-dropout regulator; adaptive bias; buffer; phase margin***

## I. INTRODUCTION

Nowadays, with the development of intelligent lifestyle, people increasingly prefer to portable devices. Due to low dropout regulator (LDR) has simple structure, low cost, low power consumption and small size, it is widely used in portable electronic products [1]. In portable products, the functions of products become versatile. At the same time, the power saving demand has been increased. Low power consumption not only means energy savings, also means extending the power cycle. In order to make the system work stability, traditional LDR adopts appropriate external capacitor to produce a zero for pole canceling in the LDR [2]. This usually requires a large capacitor, also called equivalent series resistance [3], which is not only wasting of resources but also increasing costs, while weakening the portability features of portable devices [4]. The output voltage level will change by following the load current [5], the error amplifier (EA) is used to sense the change of current and the power transistor will be driven to compensate this change. However, there is a delay between the EA reaction and the output current change, causing voltage spikes and reducing the accuracy of the circuit [6]. There are many factors that cause the delay and parasitic capacitors of the LDR is one of the main reasons [7]. It is difficult to have a good trade-off among the LDR loop bandwidth, stability and quiescent current.

Because of these challenges, in this paper, a low-voltage capacitor-less adaptively biased LDR with buffer is presented. This structure extends the loop bandwidth and improves the stability of the circuit. Since the power consumption change follows the load current [8], the circuit consumes very little quiescent current under no load conditions. Because high-precision LDR requires high loop gain [9], this design uses two-stage amplifier under low power supply voltage.

The organization of this paper is given as follows: Section Ⅱ presents the structure of the LDR and discusses its overall performance. Section Ⅲ simplifies the circuit and obtain a model to analyze the main feedback loop (MFL). Section IV presents the simulation results respectively, Section V concludes the design efforts.

## II. THE PROPOSED LDR STRUCTURE AND IT'S PERFORMANCE ANALYSIS

The generalized architecture of the proposed LDR with the structure of AB and buffer is shown in Fig.1. Schematic diagram consists of the following basic parts: the current bias circuit, bandgap reference voltage source, an error amplifier, AB structure, buffer structure, the output regulator and the feedback resistor. Current bias circuit provides high accuracy and low temperature drift current [10]. Bandgap reference provides the reference voltage $V_{REF}$ for the LDR. Error amplifier compares the feedback voltage

of the output of LDR with the $V_{REF}$ , and amplifies the difference to control the regulator, so to maintain a stable output voltage $V_{out}$. The source voltage $V_{DD}$ of LDR is 1.8V. The positive input of the differential amplifier $V_{REF}$ is 1V, and the output of LDR is 1.5V. Adaptive bias structure is introduced in the differential amplifier. Adaptive bias structure is implemented by a simple current mirror. Bias circuit provides a large bias current for EA when loads is heavy to maintain a large loop bandwidth [11]. And at light load it provides a small bias current to maintain high current efficiency. Miller capacitor $C_M$ is used to split the pole which are located at the output of EA and the output of LDR [12]. And Q-reduction capacitor $C_Q$ is used to reduce $I_{load}$ [13]. In this paper two-stage EA is used to achieve high bandwidth and high gain. Operational trans-conductance amplifier (OTA) has high gain and low bandwidth characteristic and is used as the main EA [14]. The second OTA amplifier which based on a smaller gain and larger bandwidth is mainly used to monitor the output of the LDR. The third gain stage of the LDR is power transistor $M_P$ . Since the pass transistor has a large parasitic capacitor, the EA which has a small quiescent current produces a low frequency pole at output stage of the LDR. Application of buffer isolates the high output impedance of the output stage of EA and the high load capacitor of $M_P$, pushing zero of right half plane and improving PSRR of the LDR[15]. Two-stage EA is composed of $M_0 \sim M_8$ . Bias current is composed of $M_{ab1}$ , $M_{ab2}$ , $M_{a1} \sim M_{ab3}$. Buffer is composed of $M_{ab1}$ , $M_{ab2}$ , $M_{b1} \sim M_{b1}$ , $M_{B3}$. $M_{B4}$ and $Q_0$. Miller capacitor $C_M$ connects the output of the first stage EA and the output terminal the LDR,Q-reduction capacitor connects gate and drain of $M_6$, while also connects $M_3$ and $M_4$. Under no load condition, Power transistor works in the cut-off region and the quiescent current consumption of the LDR is small. At light load condition , the rest circuit work in sub-threshold region, except the differential amplifier circuit. In this case, leakage current of $M_1$ is approximately $6\,uA$, and current is supplied by $M_{a3}$ and is almost zero, only $156\,nA$. As the load current increases to approximately $25\,uA$ , $M_P$ works into saturation region from sub-threshold region. At this point , the rest of the circuit in addition to the $M_{a3}$ located in the linear region which provides dynamic bias current for differential amplifier, and the rest of the LDR circuits are in saturation region. $M_{a3}$ in the linear region can be more sensitive to provide compensation current to the differential amplifier with the load current dynamic changes.

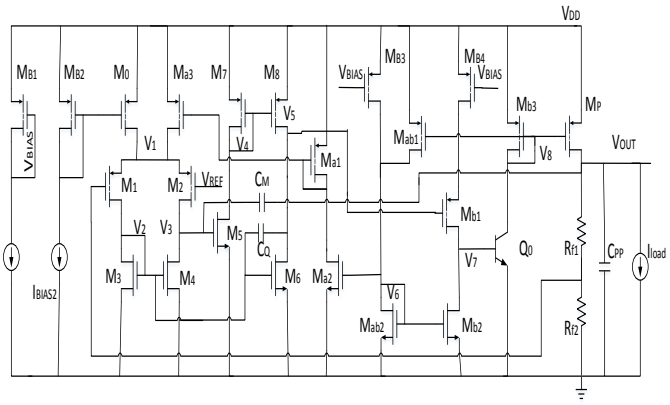



Fig.1. *Schematic of the LDR with AB and buffer structure*

$M_{ab2}$ and $M_0$ provide a fixed bias current for EA. $M_{B1}$ provides bias voltage for $M_{B3}$ and $M_{B4}$ . The implementation of adaptive bias circuit provides dynamic current for the differential circuit consists of three current mirror:( $M_{a3}$ , $M_{a1}$ ), ( $M_{ab2}$ , $M_{a2}$ ), ( $M_P$ , $M_{ab1}$ ). The ratios of current mirror are $M_{a3} : M_{a1}$ (1:1), $M_{ab2} : M_{a2}$ (40:1), $M_P : M_{ab1}$ (248:1). Fixed current combination adaptive bias current form are used in buffer structure. Among them, $M_{B3}$ and $M_{B4}$ provide fixed bias current for buffer. The current mirror consists of $M_P$ and $M_{b3}$ have the same ratio as $M_P$ : $M_{ab1}$ . $M_{b1}$ as a source follower, when it is lightly loaded in sub-threshold region. There are three main circuit poles. The first pole $P_1$ is located at the EA's output $N_1$ , The second pole $P_2$ is located at the buffer's output $N_2$ . And $P_1$ is less sensitive to the LDR's load current than the pole $P_2$ . The output pole $P_3$ is located at the LDR's output $V_{out}$ . The pole $P_1$ is mainly determined by the output impedance of EA and the equivalent capacitor of $N_1$ . The pole $P_2$ is mainly determined by the output impedance of buffer and the input capacitor of $M_P$ . The pole $P_3$ is mainly determined by the equivalent impedance and load capacitor of the output of LDR. The pole $P_3$ is more sensitive to the change of the load current than the pole $P_2$ . Larger load current would push $P_3$ to higher frequency more than push $P_2$ to high frequency. The equivalent capacitor of $N_1$ point and the output impedance of the buffer should be small, making the pole $P_1$ and $P_2$ located at very high frequency and circuit become a single pole frequency response. The output impedance of buffer is

$$R_{ob} = 1/\left[g_{mb1}(1+\beta) + g_{mb3}\right] \qquad (1)$$

$g_{mb1}$ is the transconductance of transistor $M_{b1}$. $g_{mb3}$ is the transconductance of transistor $M_{b3}$ ,β is the current gain of triode $Q_0$ .The value of β of this design

is 10. When the load current increases, $g_{mb1}$ and $g_{mb3}$ all will increase, leading to the value decrease. The load current increase also makes $P_2$ throughout the load current range located in a very high frequency, which is greater than unity gain frequency. Since the $M_{ab1}$'s $V_{DS}$ is larger than $M_P$'s $V_{DS}$, the sense current of $M_{b3}$ will change larger than the load current.

The adaptive bias structure and buffer structure also improve the slew-rate of this circuit. When the load current increase, $M_{ab1}$ and $M_{b3}$ follow $M_P$ to increase currents, thus the current of $M_{a3}$ and $M_{b1}$ increase. The increase of current of $M_{a3}$ and $M_{b1}$ will increase the collector current of $Q_0$. Gate voltage of $M_P$ will decrease when the collector current of $Q_0$ increase. At the same time,it increases a parasitic capacitor's discharge current and the slew-rate of circuit. The enhancement of slew-rate can speed up the transient response of the LDR[16].

## III. Stability Analysis of Circuit

The main feedback loop (MFL) transfer function of the LDR is presented for stability analysis , Fig. 2 is a small-signal model of the circuit main loop.

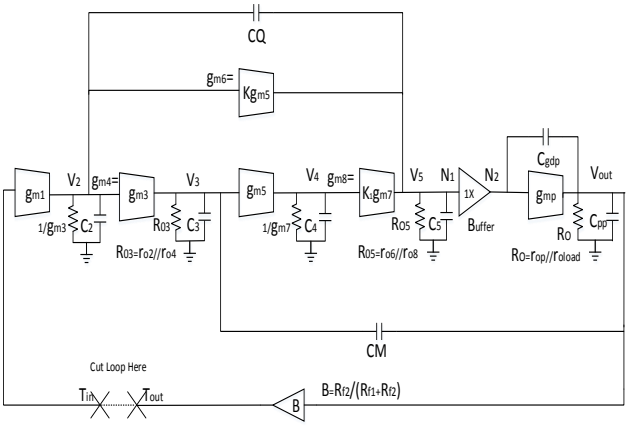



Fig. 2. *Small signal model of the LDR MFL*

B represents the circuit feedback factor. $g_{m1}$, $g_{m3}$, $g_{m5}$, $g_{m6}$, $g_{m7}$, $g_{m8}$, $g_{mp}$ represent the transconductance of each transistor. Based on the following considerations, the loop gain transfer function is presented as follows:

*1)* The parasitic capacitor from $V_2 \sim V_5$ is $C_2 \sim C_5$, in the stability analysis, the value of $C_2 \sim C_5$ is very small, and the corresponding frequency is much greater than the UGF. Therefore, the parasitic capacitor $C_2 \sim C_5$ in the calculation can be ignored. And because the power transistor $M_P$ is very large, the value of $C_{gdp}$ can't be ignored.

*2)* Power transistor $M_P$ provides the third stage gain is $Gain_3 = g_{mp} R_O$. $Gain_3$ follows the load current $I_{load}$ change. Their specific relationship is $Gain_3 \propto \sqrt{I_{load}}$.

*3)* Buffer structure with an impedance value is represented by $R_{ob}$ where in (1).

Based on the above considerations, the LDR loop gain transfer function is:

$$T(s) = \frac{T_{out}}{T_{in}} \approx A_{MFL} \times \frac{1 + a_1 s + a_2 s^2 + a_3 s^3 + a_4 s^4 + a_5 s^5}{1 + b_1 s + b_2 s^2 + b_3 s^3 + b_4 s^4 + b_5 s^5 + b_6 s^6} \quad (2)$$

With:

$$A_{MFL} = -B g_{m1} R_{o3} g_{m6} R_{o5} g_{mp} R_o \quad (3)$$

$$a_1 = \frac{C_M (g_{m6} R_{o5} g_{mp} - g_{m3})}{g_{m3} g_{m6} R_{o5} g_{mp}} + \frac{C_{gdp} g_{m3}}{g_{mp} R_{o5} R_o R_{ob}} + \frac{C_m g_{m3} R_{o3}}{R_o R_{o5} R_{ob}} \quad (4)$$

$$a_2 = \frac{C_M^2 R_{o3} + C_M C_{gdp} R_{ob}}{g_{mp} g_{m6} R_{o5}} + \frac{C_Q C_M + C_{gdp} C_M R_{o3}}{g_{m6} g_{mp}} + \frac{C_M C_Q (1 + R_{o3})}{g_{m3} g_{m6}} + \frac{C_M^2}{g_{m1} g_{m6}} \quad (5)$$

$$a_3 = \frac{C_{gdp} C_M C_Q R_{o3}^2}{g_{m3} g_{mp}} + \frac{C_M C_Q^2}{g_{m3}^2 g_{m6}^2 g_{m1}} + \frac{R_{o3} g_{m3} C_M + C_{gdp} g_{m3}}{g_{m3} g_{mp} g_{m1} g_{m6}^2} + \frac{C_M^2 C_Q}{g_{m6}^2 g_{m1} g_{mp}} \quad (6)$$

$$a_4 = \frac{C_{gdp} C_M^2 C_Q R_{o3}}{g_{mp} g_{m3}^2} + \frac{C_M^2 C_Q^2 R_{o3}}{g_{m3}^2 g_{m6}} + \frac{C_{gdp} C_M^2 C_Q R_{o3}}{g_{mp} g_{m3} g_{m6}} + \frac{C_{gdp} C_M^2 C_Q R_{o3} R_{ob}}{g_{mp} g_{m6}} \quad (7)$$

$$a_5 = \frac{C_{gdp} C_m^2 C_Q^2 R_{o3}}{g_{mp} g_{m6} g_{m3}} \quad (8)$$

$$b_1 = C_M g_{m6} g_{mp} R_{ob} R_{o5} R_{o3} \quad (9)$$

$$b_2 = C_M C_Q (R_{o3} + R_{o5}^2) + C_M C_{gdp} (R_o R_{ob} + R_{o3} R_o + 1) + C_M C_{PP} + C_{PP} C_{gdp} R_o R_{ob} \quad (10)$$

$$b_3 = \frac{C_M C_Q C_{gdp} (R_o R_{ob} + R_{o5} R_{o3})}{g_{m3}} \quad (11)$$

$$b_4 = \frac{R_{o3} R_o C_Q C_{gdp}^2 C_M + R_{o3}^2 C_M^2 C_{gdp} C_Q}{g_{m3}} \quad (12)$$

$$b_5 = \frac{R_{o3}R_{ob}R_oC_Q^2C_{gdp}C_MC_{PP}}{g_{m3}} + \frac{R_{o5}^2R_oC_M^2C_{gdp}C_QC_{PP}}{g_{m3}} + \frac{R_{o3}^2R_oC_{pp}^2C_{gdp}C_QC_M}{g_{m6}} \quad (13)$$

$$b_6 = \left(C_M^2C_Q^2C_{gdp}C_{pp}R_{o3}^2R_{ob}R_oR_{o5}\right)/g_{m3} \quad (14)$$

From (2), (3) and (9), The unity gain bandwidth can be obtained as follows $w_{UGF} = Bg_{m1}/C_M$ , the denominator is 6 order polynomials, showing that there are six poles. Poles which varies with load impedance $R_o$ can be clearly seen (10) ~ (14). Under the light load conditions, though $g_{mp}$ is small, the value of $R_o$ is large. Because of $g_{mp}R_o \propto 1/\sqrt{I_{load}}$ , under the light load conditions, the DC gain is larger and PSRR is larger as well. Large PSRR means smaller ripple.

When the load current $I_{load} = 0$, $g_{mp}$ is small, and the leakage current of transistor $M_P$ is least. Buffer is used to reduce the output impedance. The value of $C_5$ can be decreased by reducing the size of $M_{b1}$ at $I_{load} = 0$ which UGF is located at higher frequency and better phase margin is obtained. When $I_{load}$ increases, $g_{mp}$ also increases and the second pole also increases. The phase margin and stability become better.

Under no load condition, the quiescent current of this LDR consumption of 163.4uA. At this time, UGF is 1.57MHz and phase margin is 54°. With the increase of load current, UGF and the phase margin also increases. When the load current at maximum is 100mA, the quiescent current is 500uA, and the UGF is 1.66MHz. Compared to no buffer structure at the LDR circuit, UGF increase to 0.46MHz.

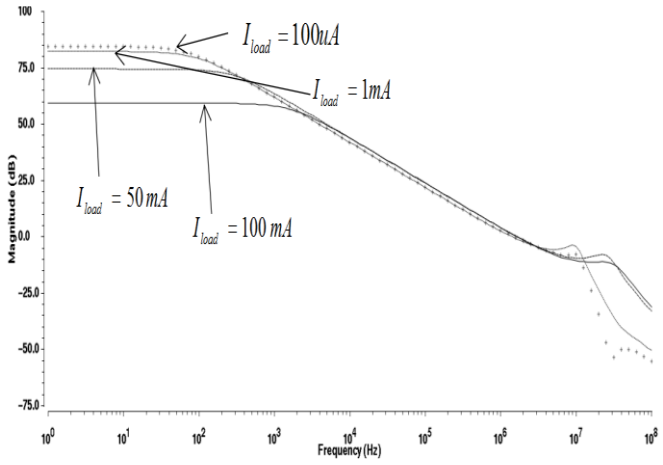



Fig. 3. *The MFL simulation amplitude waveform*

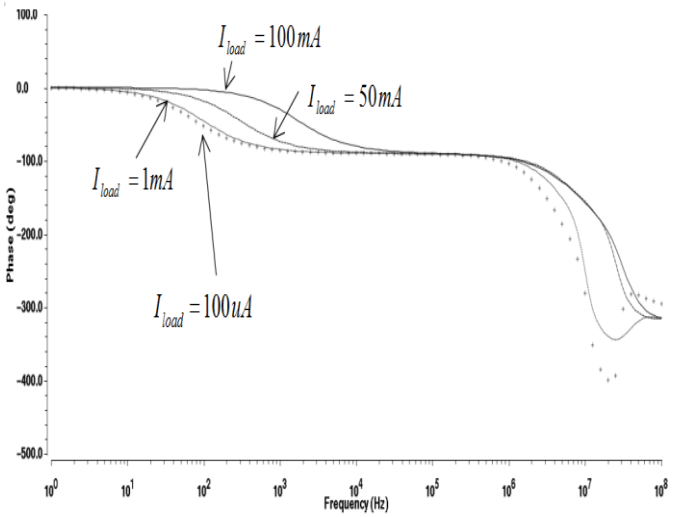
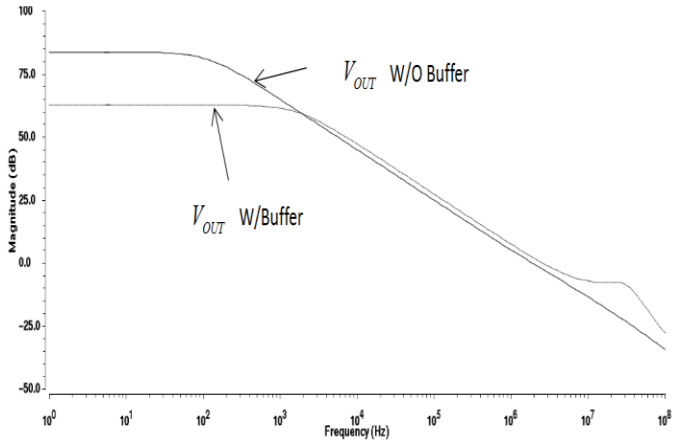
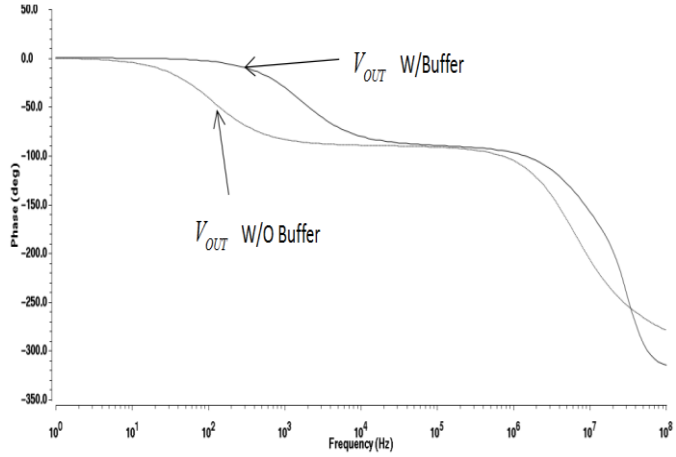



Fig. 4. *The MFL simulation frequency waveform*




(a)




(b)

Fig .5. *The frequency responses waveform at 100mA load with and without buffer: (a) amplitude waveform (b) frequency waveform*

The simulations is shown in Fig. 3 and 4 to illustrate the loop gain of the frequency response curve. It can be seen from figure 6, the first and second pole are pushed to the outside of the unit gain bandwidth. When the load current changes from 100uA to 100mA, all phase margin is larger than 45°. When the load current is 100uA, the phase margin is 54 °, gain is 85.24dB; when the load current is 100mA, the phase margin is 77° and gain is 59.03dB.

It can meet the gain requirements of the LDR's EA and achieve good stability performance.

In Fig.5, it's shown that after adding buffer structure, the gain becomes smaller. The reason is that the buffer structure reduces the output impedance. It is generally understood that amplifier gain can be written as the $A_v = g_m R_o$. Compared to the no buffer circuit, the gain with buffer circuit become smaller for the $R_o$ become smaller. In Fig.6, it is shown that the LDR with buffer structure phase margin is higher than that without buffer structure. For the reason that $R_o$ becomes smaller, the corresponding pole is pushed to outside of unit gain bandwidth which is located at the frequency that higher than without buffer structure. So this structure is more stable.

## IV. Simulation Results

The proposed LDR with buffer and AB structure is designed by using a standard 0.11- um CMOS process. The value of the compensation capacitor and Q-reduction capacitor are both 10 pF. The parasitic capacitor of the LDR is assumed to be 100 pF in the simulations. Table I shows the performance of the proposed LDR with buffer and AB structure.

TABLE I. The Summary of The LDR Performance

| Technology | HHGRACE 0.11-um 2P4M CMOS |
|---|---|
| $V_{DD}$ | 1.8V-5V |
| $V_{REF}$ | 1V |
| $V_{out}$ | 1.5V |
| $I_{load}$ | 100uA-100mA |
| $C_{PP}$ | 100pF |
| $C_M$ , $C_Q$ | 10pF,10pF |
| Line Reg.@100mA | 1.0mV/V |
| Load Reg.@1.8V | 6.01uV/mA |
| Line Tran. $\Delta V_{out}$ (2.3-2.0V@100mA) | -11mV/+1mV 2.5us |
| Load Tran. $\Delta V_{out}$ (1-50mA@1.8V) | -553mV/+191mV 0.7us |
| PSR@1kHZ,1mA | -77.64dB |
| PSR@1kHZ,50mA | -65.61dB |
| PSR@100kHZ,1mA | -22.02dB |
| PSR@100kHZ,50mA | -24.26dB |

As shown in Table I, the range of power supply $V_{DD}$ is between 1.8 and 5V, the EA's positive input $V_{REF}$ is 1V, and the LDR's output $V_{out}$ is 1.5V. The maximum load current is 100mA. For dynamic performance, the line regulator is 1.0mV/V at 100mA load current and the load regulator is 6.01uV/mA at 1.8V power supply. When $I_{load}$ is 100mA $V_{DD}$ is be changed from 2.3V to 2.0V in 2.5us and the transient error voltage of $V_{out}$ is within 11mV. The load transient response is measured with load current from 1mA to 50mA at $V_{DD}$ =1.8V, and the undershoot (overshoot) voltage is 553 mV (191mV). At 1Hz frequency, the light load current have better PSRR than heavy load. But the PSRR with 50 mA is better than that with 1 mA under 100kHz. The reason is that the influence of parasitic capacitor and load capacitor become remarkable in high frequency.

## V. Conclusions

In this paper, the LDR with buffer and AB structure is proposed. The AB structure is sensitive to the change of load current and increase the accuracy of the LDR. The buffer structure attenuates the output resistance which drives the power transistor and pushes the pole at the gate of the power transistor to higher frequency. The AB structure and buffer structure also improve the slew-rate and speed up the transient response of the LDR. Experiment results show that the proposed LDR has good stability and PSRR. The AB structure improves the transient response of the LDR. Simultaneously, it can ensure the enough phase margin and maintain the stability of the LDR under heavy load conditions. Buffer structure further improves the stability of the LDR under the full range of load currents. And internal compensation capacitor can be as small as 10pF without external capacitor. Capacitor-less LDR with adaptively biased and buffer structure can reduce the chip area of portable devices and have more stable performance.

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