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Comparative Study Of Multi Layer Nano Ribbon In Nano Scale Region

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***Abstract*—In the growing age of VLSI Interconnects many scientists have proven that graphene nano-ribbon (GNR) interconnects are excellent candidate for interconnection. In this work comparative study has been made on single conductor and multi conductor models of graphene nano-ribbon in terms of propagation delay at 16 nm and beyond 16 nm. For the work driver-interconnect-load system has been used using FinFETs. The work has been carried out in three operating regions and for different parallel connected devices.**

Keywords—Single and Multi conductor models, Graphene nano ribbon, FinFET, Interconnect, Propagation delay.

I. INTRODUCTION

With the continuously increasing demand for VLSI interconnection researchers with their brilliant work have been suggested that the VLSI interconnects made from graphene can fulfill the demand of modern high speed VLSI circuits [1]. In [2] Giem showed that graphene is a monolayer made up of carbon atoms and exists is the form of ribbon. Giem also mentioned that graphene acts as a mother of carbon nanotube interconnects.

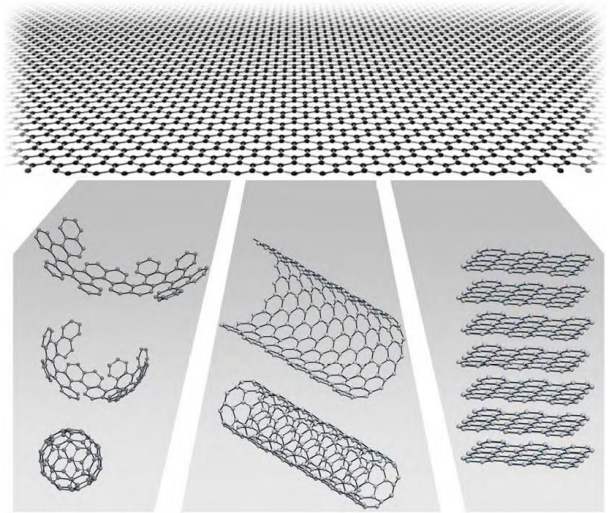

Figure .1.View of Graphene as a 2D building material and other structures made by graphene layer [2].

This paper carries comparative analysis of propagation delay of a driver-interconnect-load (DIL) system which is using graphene as an interconnect and FinFET as a driver and load circuit. Single and multi conductor models of graphene nano-ribbon have been used for the study.

II. METHODOLOGY USED

A. Interconnect model

The equivalent models for graphene nano-ribbon interconnect which have been used in the work are shown in fig.2.

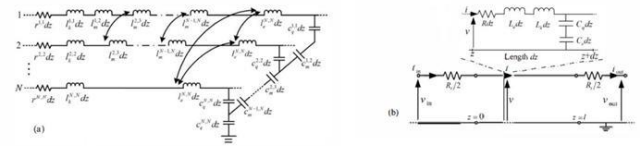

Figure .2. Equivalent model (a) Multi-conductor (b) Single conductor [3]

For the multi conductor model authors in [4][5][6] have given the expressions which have been used to calculate quantum resistance, quantum and electrostatic capacitance, kinetic and electrostatic inductance.

$$R_Q = (h/2q^2)/N_{ch}N_{layer} = 12.94\ k\Omega/\ N_{ch}N_{layer} \quad (1)$$

$$C_Q = N_{ch}N_{layer}\ 4q^2/hv_f = N_{ch}N_{layer} * 193.18\ aF/\mu m \quad (2)$$

$$C_E = \varepsilon_0 * w/d\ aF/\mu m \quad (3)$$

$$L_K = (h/4q^2v_f)/\ N_{ch}N_{layer} = 8.0884/\ N_{ch}N_{layer}\ nH/\mu m \quad (4)$$

$$L_E = \mu_0 * (d/w)\ nH/\mu m \quad (5)$$

Where, N_{ch}= number of conducting channels in one layer, N_{layer}= number of GNR layers, h = Plank's constant, q = electronic charge, and v_f= Fermi velocity for GNR.

And for the single conductor model authors have given the expressions for resistance, capacitance, and inductance in [7].

$$R_{ESC} = 12.94\ k\Omega/\ \lambda\ N_{ch}N_{layer} \quad (6)$$

Where λ is mean free path.

$$L_{ESC} = L_K + L_E \quad (7)$$

$$C_{ESC} = (C_Q + C_E)^{-1} \quad (8)$$

B. Driver-interconnect-load model

. The DIL system which has been used in this work carries FinFET as a driver and load circuit. Three forms of FinFETs have been used, namely short gate FinFET, independent gate FinFET, and low power FinFET.

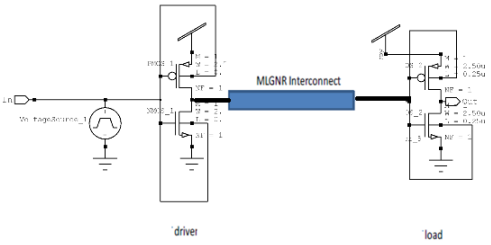

Figure .3.Driver- interconnect-load system (DIL) using SG FinFET driver-load stage [8].

III. RESULT AND ANALYSIS

Results which have been shown in this section carried out using TSPICE 14.0. The three different operating regions which have been used in the work are super-threshold region, near threshold region, and sub-threshold region. Graphene nano-ribbon with 3, 10, and 20 layers has been used and three types of FinFETs have been used with different number of parallel devices which is shown by M.

Agnihotry and Agarwal in [8] have calculated the propagation delay for single and multi conductor graphene nano- ribbon at 16 nm. The same effect has been studied beyond 16 nm in this paper and comparison has been done with the results at 16 nm.

From my previous work it is clear that all the three types of FinFETs show similar result in terms of propagation delay beyond 16 nm.

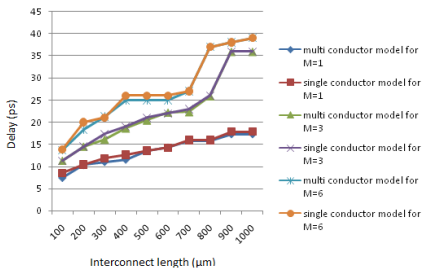

Figure .4.Effect of length on delay for DIL system in super threshold region for graphene layer = 3.

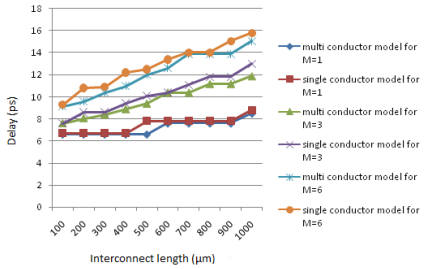

Figure .5.Effect of length on delay for DIL system in super threshold region for graphene layer = 10.

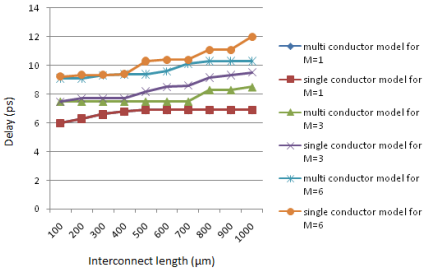

Figure .6. Effect of length on delay for DIL system in super threshold region for graphene layer = 20

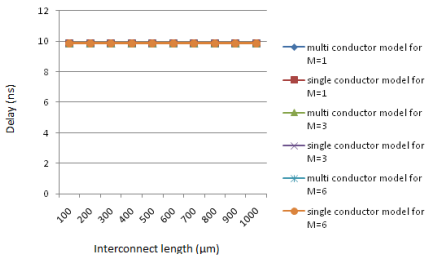

Figure .7. Effect of length on delay for DIL system in near threshold and sub threshold region for graphene layer = 3

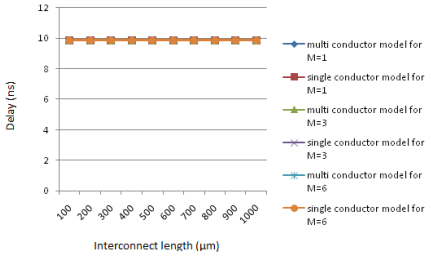

Figure .8. Effect of length on delay for DIL system in near threshold and sub threshold region for graphene layer = 10

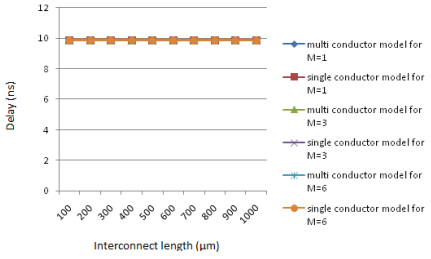

Figure .9. Effect of length on delay for DIL system in near threshold and sub threshold region for graphene layer = 20

Fig.4 to 6 shows the effect of length on delay for DIL system beyond 16 nm. Results have been taken for both multi and single conductor models of graphene nano-ribbon. And Table.1 to 3 shows the improvement in delay for single and multi conductor models at 16 nm and beyond 16 nm.

From fig.7 to 9 it is clear that the value of propagation delay has no change in near threshold and in sub threshold regions.

Table.1 Percentage improvement of single and multi conductor GNR beyond 16 nm over 16 nm node for layer = 3

% improvement of delay at GNR layer = 3						
	Multi conductor model of MLGNR beyond 16 nm vs multi conductor MLGNR at 16nm			single conductor model of MLGNR beyond 16 nm vs single conductor MLGNR at 16nm		
	M=1	M=3	M=6	M=1	M=3	M=6
SG FinFET DIL	99.47	99.51	99.57	99.39	99.53	99.60
IG FinFET DIL	99.75	99.65	99.60	99.71	99.65	99.64
LP FinFET DIL	99.76	99.66	99.66	99.74	99.65	99.66

Table.2 Percentage improvement of single and multi conductor GNR beyond 16 nm over 16 nm node for layer = 10

% improvement of delay at GNR layer = 10						
	Multi conductor model of MLGNR beyond 16 nm vs multi conductor MLGNR at 16nm			single conductor model of MLGNR beyond 16 nm vs single conductor MLGNR at 16nm		
	M=1	M=3	M=6	M=1	M=3	M=6
SG FinFET DIL	99.47	99.66	99.70	99.53	99.68	99.73
IG FinFET DIL	99.75	99.76	99.73	99.77	99.76	99.74
LP FinFET DIL	99.78	99.76	99.77	99.71	99.77	99.77

Table.3 Percentage improvement of single and multi conductor GNR beyond 16 nm over 16 nm node for layer = 20

% improvement of delay at GNR layer = 20						
	Multi conductor model of MLGNR beyond 16 nm vs multi conductor MLGNR at 16nm			single conductor model of MLGNR beyond 16 nm vs single conductor MLGNR at 16nm		
	M=1	M=3	M=6	M=1	M=3	M=6
SG FinFET DIL	99.52	99.66	99.69	99.37	99.38	99.72
IG FinFET DIL	99.76	99.75	99.74	99.80	99.78	99.74
LP FinFET DIL	99.80	99.76	99.77	99.93	99.93	99.76

IV. CONCLUSION

From the study in has been concluded that the performance of driver-interconnect-load system is better when multi conductor model of graphene nano-ribbon interconnect is used. And it has also been concluded that performance of driver-interconnect-load system will become much better if multi conductor model with large number of graphene layers are considered.

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