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An Efficient Congestion Aware Adaptive Routing Techniques in Dram

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Abstract—The power dissipated by system-level buses is the largest contribution to the global power of complex VLSI circuits. Therefore, the minimization of the switching activity at the I/O interfaces can provide significant savings on the overall power budget. This paper presents innovative encoding techniques suitable for minimizing the switching activity of system-level address buses. In particular, the schemes such as full inversion, even inversion and odd inversion target the reduction of the average number of bus line transitions per clock cycle. Experimental results, conducted on address streams generated by a real Field Programmable Gate Array (FPGA), have demonstrated the effectiveness of the proposed methods. It can reduce the power consumption and improvement in performance and throughput when compared to existing system.

Keywords—FPGA, power, area, performance, ETI, PaCC.

I. INTRODUCTION

More number of non-volatile flip flops and registers are used.it requires more amount of space and energy for power consumption. In existing system processors contain capacitor for easy drain off the power supply .As the system does not requires any external backups. Non-volatile processors require more time to initiate the system and data is erased when supply is OFF and that condition requires more power dissipation.

II. OVERVIEW

The processor is implemented for area impact and redundancy problem .It reduces the average number of bus line transition due to cyclic process.

A. PaCC Design

Generally processor ratio is analysed by using compress and compare scheme .By using this parallel compare and compress scheme, compression ratio of the data level is reduced. But it has a problem due to transmission of data bit into the processor. Due to transmission of large number of data bit into the processor, collision occurs. This problem is rectified in collision avoidance scheme. Here a technique of run length encoder is used to reduce redundancy of the bit level.

B. Run length encoder(RLE)

A data bit can be reduced from 16k to 2k level.

0000 1111 0000

0 1 0

By using run length encoding only continuous zero and one can be reduced. If there is a mismatch of bit level 101010 –data bit cannot be compressed by using RLE method. So inversion technique is involved for reducing the data bit level.

III. Proposed Method

METHOD FOR REDUCING CONGESTION

A. Embedded Transition Inversion (ETI) ENCODER

From Embedded Transition Inversion (ETI) encoder four inversion techniques is involved to compress the data bit.

- Full inversion
- Odd inversion
- Even inversion
- Zero inversion

Inversion techniques take place due to compression of data length. For example full inversion requires inverting all one as zero and zero as one.

Even inversion For example 01010101 here even inversion can be take place

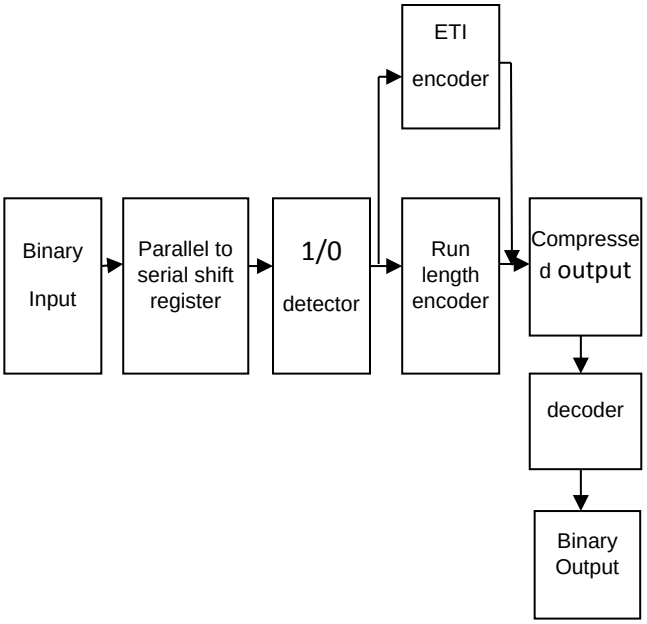
Even 1 0

0 1 0 1 0 1 0 1

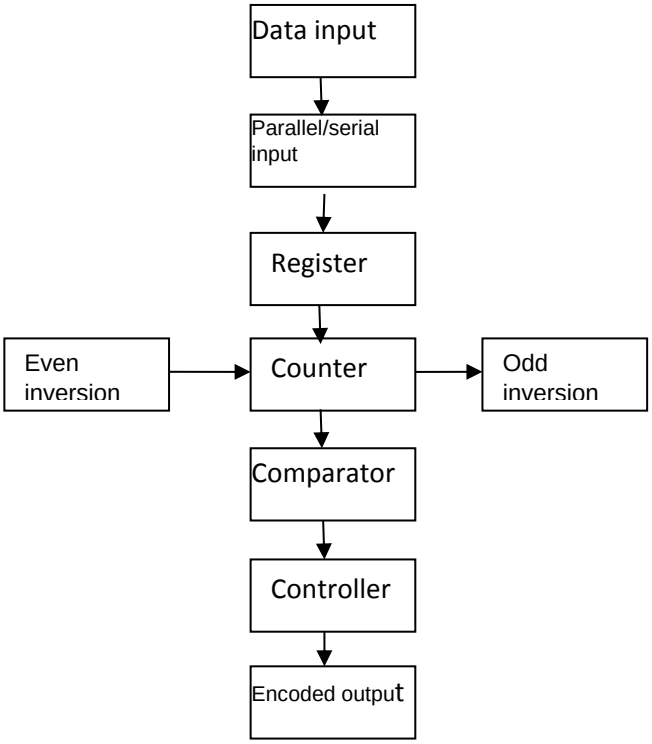
0 0 0 0

In this inversion 1—0(changed) one can be converted to zero. Like that for odd inversion also only odd term of data bit is changed and length of bit level is reduced.

B. **BLOCK DIAGRAM**

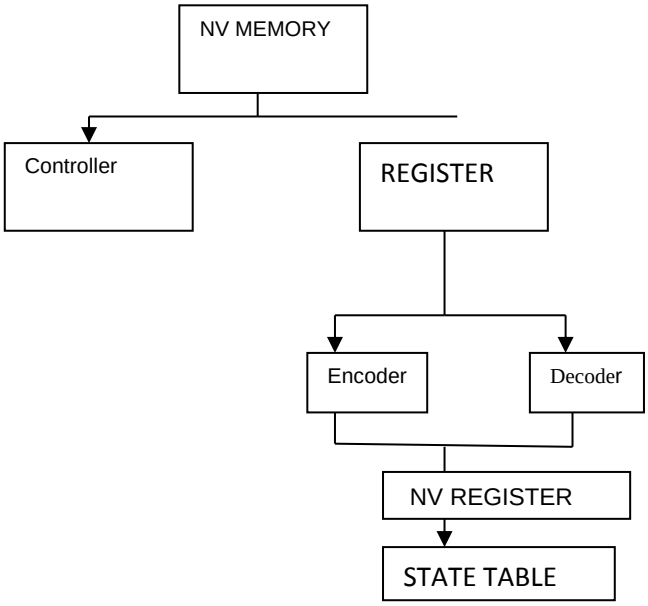


C. **ETI ARCHITECTURE**



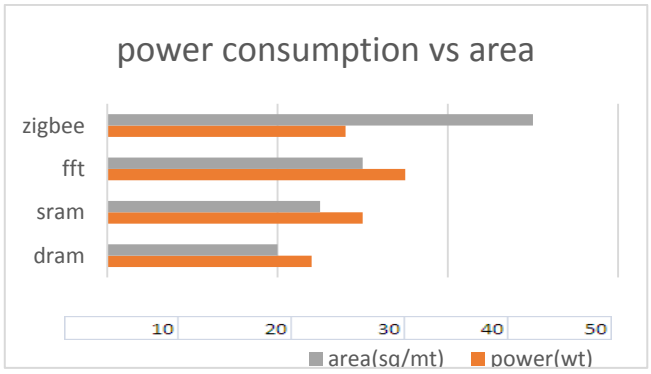
ETI encoder has inversion technique. This technique is used to compress the data bit level. The graphical chart is refer to reduction of the area and power consumption.

D. **Non-volatile processor**



IV. Results and Discussion

A. Analysis report for power consumption

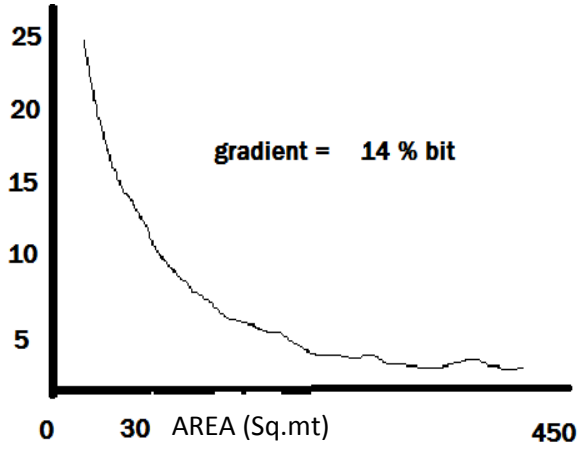


Area reduction in parallel compare and compress scheme is achieved but few error occurs due to large number of data is transmitted at the same time instant.

Area reduction=Area total-Area compressed

From that over all area is reduced due to reduction of register and flip flops.

B. Gradient Chart

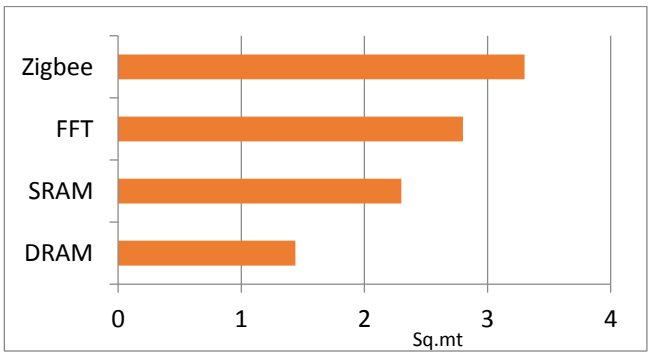


From the evaluation PACC leads to compression of the data bit level. It is implemented in real time system for more memory space and less power consumption. From the chart it is observed that area is reduced to bit level of 14%.

C. Area reduction

From PACC method area is compressed by using design compiler. Based on reduction only 23.4% to 27% is reduced .By using an inversion techniques scheme area is reduced up to 33% to 39% .It is efficient and collision problem is reduced.

D. Area analysis chart

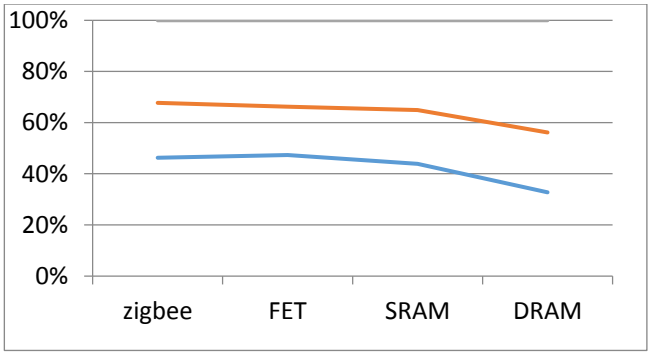


From the chart it is observed that the area is reduced maximum for DRAM and it 1.4 sq meters.

E. Codec performance level

The run length encoder and decoder plays role in PaCC method but it is not efficient for reduction of data bit level .So inversion scheme exhibits better performance in reduction of bit level.

F. Power and area minimization chart



Area is minimized up to 33% and power consumption is reduced up to 42% for DRAM.

V. CONCLUSION

Non Volatile processor reduces power consumption and area size .The cost of chip is also reduced. From advanced codec level of parallel compare and compress scheme it reduces the number of flip flops .According to this technique, power consumption and bit level compression cannot be reduced by using congestion aware techniques .It reduces traffic due to data transmission and glitches is avoided.

Network level data transmission causes congestion problem. It can be avoided by using congestion aware techniques and inversion is used to reduce that data bit level. Area is reduced up to 33% and power consumption is reduced up to 42%.

VI. Acknowledgment

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VII. REFERENCES

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