Journal of Multidisciplinary Engineering Science and Technology (JMEST)
ISSN: 3159-0040
Vol. 1 Issue 5, December - 2014

Designing and simulation of a new Low voltage-Low power current mode Devider circuit

Forough Pakray
Department of Electronic Engineering, Omidiyeh Branch, Islamic Azad University, Omidiyeh, Iran
f_pakrai2006@yahoo.com

***Abstract*— A general framework for designing current-mode CMOS analog multiplier circuit based on the cascade connection of a geometric-mean circuit and a divider is presented. In this paper, novel current-mode analog squarer circuit based on a pair of voltage-translinear Loop is presented. The proposed circuit is designed in 0.18 µm standard CMOS technology.Simulation result using HSPICE that verify the functionality of circuit with 1 V supply is presented. The circuit can find application in the implementation of wide range of analog systems, Fuzzy and Neural Network circuits.**

***Keywords*— Analog processing circuit, Translinear loop, Squarer, Low Voltage.**

I. INTRODUCTION

Squaring circuit is a mathematical function that is widely used in communication system and measurements such as frequency doublers, peak amplitude detector, and analog multiplier [11]. Squaring circuits are also widely used in other practical applications such as RMS-to-DC converters in instrumentation and non-linear signal generation in analog signal processing. Low power supply consumption has become one of the main issues in electronic industry for many product areas such as cellular telephones, portable computers, neural network, wireless sensor network, and biomedical implants. Analog circuit design has received wide attention due to the supply voltage scaling down and their potential of lower power consumption [8, 10 from 12] and they are used in the fields of analog signal processing and parallel-computing neural or fuzzy systems. These applications usually require squarer circuits to cancel non-linearity or to implement modulators or aggregation operators [3-6].

Several techniques to design CMOS squarer circuits have been proposed in the literature.The first approach is to use the current-mode square root and squarer circuit based on the square-law characteristics of MOS transistors operated in the saturation region.[3] However, the power consumption by this approach is large; the square circuit requires bias currents for all input signals to make MOS transistors operate in the saturation region. The second approach is to use translinear principle of MOS transistor operated in the saturation or subthreshold region. [1, 2]

The translinear principle, introduced by Barry Gilbert in 1975 [I], is one of the most important circuit theory contributions in the electronics era. In its original formulation, the translinear principle provides a simple and efficient way to analyze and synthesize nonlinear circuits based on bipolar junction transistors (BJTs). Due to their exponential characteristics, the translinear principle can be extended to MOS transistors operating in saturation. This approach has the advantage of low power consumption.

In this paper we proposed a new low-voltage squarer circuit base on the properties of translinear loop which is work in saturation region. The proposed circuit work with a single power supply 1V which is lower than previous proposals and make it suitable for low-voltage and portable applications.

Section II reviews the properties of translinear loops. The proposed squarer circuit is described in section III and simulation result is presented in section IV. Conclusion is presented in section V.

II. VOLTAGE TRANSLINEAR LOOPS

Consider, for instance, the circuits of Figs. 1a and 1b. They represent a four-transistor voltage-translinear loop in stacked and up-down topology, respectively, with two MOSFETs connected clockwise and another pair connected counterclockwise. Applying the KVL, the following expression is obtained for both cases:

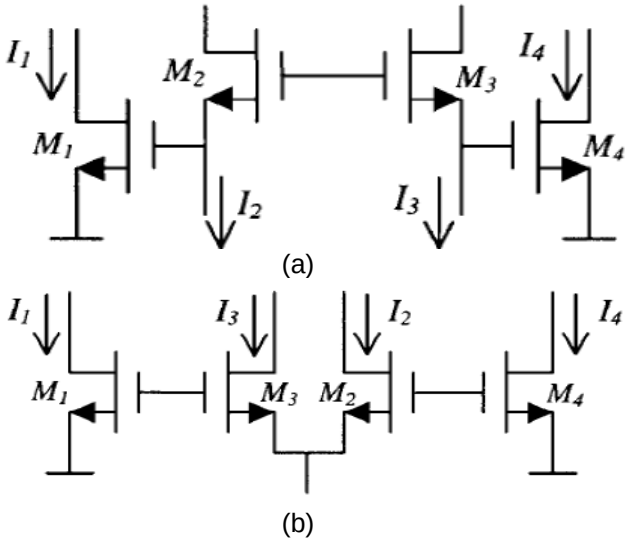

Fig 1. Voltage translinear-loop (a) Stacked Topology (b) Up-down topology

$$V_{GS1} + V_{GS2} = V_{GS3} + V_{GS4} \quad (1)$$

And replacing $V_{GS} = V_{th} + \sqrt{\frac{2I}{\mu C_{ox}\frac{W}{L}}}$ and assuming equal MOS transconductance factors and threshold voltages, the following expression is obtained:

$$\sqrt{I1} + \sqrt{I2} = \sqrt{I3} + \sqrt{I4} \quad (2)$$

Hence, several nonlinear current-mode functions can be implemented by properly injecting such currents. For instance, if we force

$$I3 = I4 = \frac{I1+I2+2I5}{4} \quad (3)$$

Being I_5 a certain current, after squaring both sides in (3) and rearranging, currents I_1 , I_2 and I_5 become related by

$$I5 = \sqrt{I1\, I2} \quad (4)$$

Therefore, a geometric-mean circuit is obtained if I_1 and I_2 are the input currents and the output current is a copy of I_5 .Alternatively, a squarer/divider is obtained if the output is a copy of I_2 and the inputs are I_1 and I_5 . The simplest way to force (4) is to use the well-known structure of Fig. 2. However, the diode-connected MOSFET of the current mirror precludes very low voltage operation due to the stacking of two diode-connected transistors.

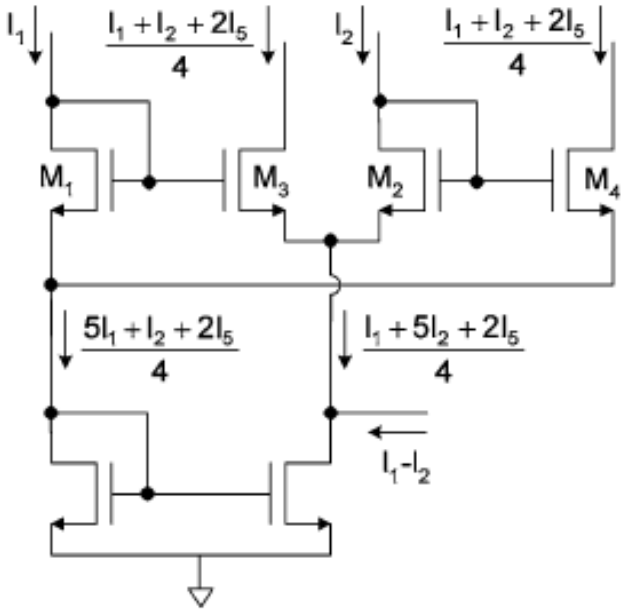

Fig. 1 The square/Divider using stack loop

III. THE NEW LOW-VOLTAGE SQUARER CIRCUIT

Equation (4) can be alternatively implemented using the novel topology of Fig. 3. Now a FVF, formed by transistors M_1 and M_{F1}, sets the proper reference dc voltage at the loop nodes. An advantage of this structure is that the source of M_1 is a very low impedance node, so that voltage at this node is kept essentially constant regardless of the input and output current.

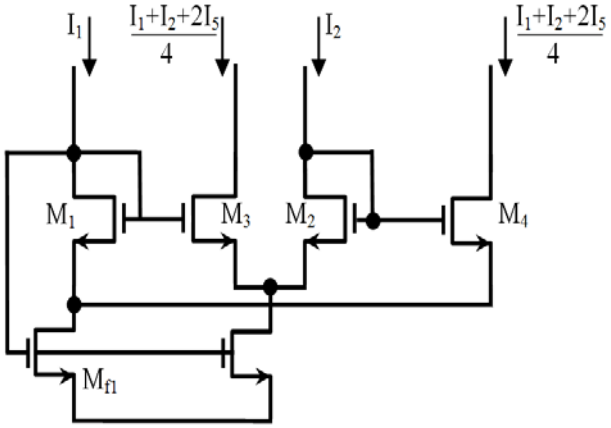

Fig. 2 The proposed low-voltage squarer circuit

The minimum supply voltage is limited by the path formed by I_b, M_1 and M_{F1} so the minimum supply voltage is

$$V_{DD\,min} = V_{GSF} + 2V_{DSbsat} \quad (5)$$

where V_{GSF} is gate-source voltage of M_{F2} , V_{DSbsat} is the minimum voltage drop in current source I_b and can be as small as 0.1V in 0.18µm CMOS technology, V_{th} =0.55 V for NMOS so,

$$V_{DD\,min} = V_{th} + 3V_{DSbsat}$$

$$V_{DD\,min} = 0.55 + 3 * 0.1$$

$$V_{DD\,min} = 0.85V$$

We have selected V_{DD}=1V in order to have an appreciable voltage swing.

IV. SIMULATION RESULT

The squarer circuit depicted in fig.3 was laid out in standard 0.18µm CMOS technology. Post layout simulations from extracted circuit were performed for a 1 V single power supply voltage using HSPICE and level 49 parameters (BSIM3V3).

Fig.4 shows SPICE simulation of the squarer circuit where we applied a constant DC current as I_1 and a triangular current for I_2.The result is showed by I_{OUT} .

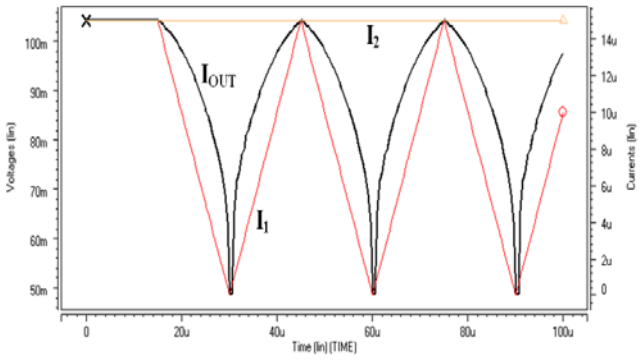

Fig. 4 Simulation result of proposed squarer

V. CONCLUSIONS

A new, Low-voltage current squarer circuit based on properties of a translinear loop is described. The proposed circuit works with a single 1V power supply

which makes it suitable for designing low-voltage multiplier/divider.

VI. ACKNOWLEDGMENT

This paper was resulted from research proposal entitled “Designing and simulation of a new Low voltage-Low power current mode Devider circuit” which is supported by "Department of Electronic Engineering, Omidiyeh Branch, Islamic Azad University, Omidiyeh, Iran".

References

[1] A.Lopez-Martın, A. J. and Carlosena, A., “A systematic approachto the synthesis of square-root domain systems,” In Proc. of IEEEInt. Symp. on Circuits and Systems, Orlando, FL, vol. V, 1999,pp. 306–309.

[2] Liu, S. I., “Low voltage CMOS four-quadrant multiplier.” Electron.Lett. 30(25), pp. 2125–2126, December 1994.

[3] Saxena, N. and Clark, J. J., “A four-quadrant CMOS analogmultiplier for analog neural networks.” IEEE Journal of Solid- State Circuits 29(6), pp. 746–749, June 1994.

[4] Han, G. and Sanchez-Sinencio, E., “CMOS transconductance multipliers: A tutorial.” IEEE Transactions on Circuits and System II 45(12), pp. 1550–1564, December 1998.

[5] Gai, W., Chen, H. and Seevinck, E., “Quadratic-translinear CMOS multiplier-divider circuit.” Electron. Lett. 33(10), pp. 860–861, May 1997.

[6] Gilbert, B., “Translinear circuits: A proposed classification.” Electron. Lett. 11(1), pp. 14–16, January 1975.

[7] . Seevinck, E. and Wiegerink, R. J., “Generalized translinear circuit principle.” IEEE Journal of Solid-State Circuits 26(8), pp. 1098–1102, August 1991.

[8] . Gilbert, B., “Translinear circuits: An historical overview.” Analog Integrated Circuits and Signal Processing 9(2), pp. 95–118,March 1996.

[9] Eskiyerli, M. and Payne, A. J., “Square Root Domain filter design and performance.” Analog Integrated Circuits and Signal Proc. 22, pp. 231–243, March 2000.

[10] Lopez-Martın, A. J. and Carlosena, A., “Geometric-mean based current-mode CMOS multiplier/divider.” In Proc. of IEEE Int. Symp. on Circuits and Systems, Orlando, FL, vol. I, 1999,pp. 342–345. [11] S. Kazemi Nia, A. Khoei, Kh.

[11] P. Prommee and K. Dejhan, “A Squaring circuit using MOSFET,” 17th Electrical Engineering Conference, 1994.