Journal of Multidisciplinary Engineering Science and Technology (JMEST)
ISSN: 2458-9403
Vol. 8 Issue 9, September - 2021

Chronometer Established By The 555 Oscillator

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***Abstract*—Under the developed society of industry and business, "How to control the time accurately?" is a very important work. Therefore, the chronometer established by the 555 oscillator is essential among industry, business and dally life. [example]; the automation of products in factory must control the required time accurately for every equipment processes. The Pharmaceutical factory of biochemistries needs to control the catch time accurately for producing every kinds of the medicine. Upon the military, we need to control the flying time of missiles accurately.**

This research paper can be divided into two parts. The first part is 555 astable multistage oscillator. It can change the electric circuit both charging state and discharging state by using diodes in order to output the digital pulse of equal duty time. The second part is the chronometer of minute and second that is composed of two counters of modulus 60. When the digital pulse that comes from the oscillator of first part transfers to the second part, then the second part will start the chronometer of minute and second.

Keywords—astable multistage oscillator, equal duty time, digital pulse, counter, chronometer

I. Introduction

This astable multistage oscillator in part I is one kind of mixed signal by analog and digital. It is often used to control time (delay or clock) and function generated in wave type. It is very cheap and high accurately. The second part is the chronometer of minute and second. It is a collocation by a decimal counter and other logic ICs. Then, it becomes two chronometers of mode 60.The second part is a logic circuit completely. This research paper is to use the analog circuit and digital logic circuit interaction, no longer need a function generator.

II. Literature Review

There are some research examples about the chronometer by oscillator in previous years. In the literature [1], Chen Jianchen graduated in his master's thesis research on "Hartley oscillator of low-phase noise and the design of voltage- controlled oscillator with double frequency band". The advantage of this paper is that simple inductors and capacitor can create high frequency oscillators. The disadvantage of this paper is that these inductors are prone to mutual inductance and cause frequency instability. In the literature [2], Li Hongjun graduated in his master's thesis research on "The design of voltage- controlled oscillators for low voltage and wide frequency band". The advantage of this paper is that the oscillation frequency can be flexibly adjusted through a variable control voltage. The disadvantage of this paper is that the circuit with variable control voltage is very complicated and error-prone. In the literature [3], Wang Shensi graduated in his master's thesis research on "The design of the voltage- controlled oscillator and the effect of base noise on the voltage- controlled oscillation". The advantage of this paper is to simplify the variable control voltage. The disadvantage of this

paper is that it also generates noise interference, which is annoying. In the literature [4], You Haozheng graduated in his master's thesis research on "Time-of-flight laser ranging timer characteristics measurement". The advantage of this paper is that the analogy of the laser range finder to be as a basis for the timer can simplify the construction. The disadvantage of this paper is that the error of the laser range finder is not small.

III. Principle Explanation

(1)The total electronic components used by this research paper have ①logic IC: 74LS90*4, 74LS47*4, 74LS08*2, 74LS32*2, logic IC555*1 ② electronic resistance 200Ω(1/4w)*2, 5kΩ(1/4w)*2, 2.2kΩ*2 ③ capacitance 100μF(50V)*1, 0.01μF*1 ④ diode (numbering:IN4001)*1 ⑤ common anode seven-segment LED monitor (small type)*4 ⑥ 3-point 2- segment sliding switch*1 ⑦LED light*1 ⑧circuit board*1 (numbering EIC-1106)

(2)The total wiring diagram of this research paper is shown as figure (1)

(3)The detail wiring diagram of 555 astable multistage oscillator is included in figure (1). Figure (2) is the path through which the current flows in charging process.

(4)In figure (2), the current path is from point e to point a. Because $R_B = R_{B1} + R_{B2} = 7.2k\Omega >> R_D = 5\Omega$, then, the current passes through the abcd path instead of the R_B path. At the same time, the voltage of output $V_3(V_{out})$ is direct current bias V_{CC} ($V_3=V_{CC}$). Because the charging process in figure (2) is the first time, then its required time is transient. We denote the time by t_0 (seconds).

(5)The electric current path in figure (3) is discharging process. Because the diode is retrograde, therefore the current path is closed. The electric current can't flow through cb path. At the same time, the output voltage V_3 (V_{out}) is low potential "ϕ" ($V_3=V_{out}=0$) and its time range is t_1 (seconds)

(6)According to the electric resistance of discharging path in figure (3), we can calculate the discharging time t_1 as follows:

$$t_1=R_B*C*\ln 2= (7.2x10^3\Omega)* (100x10^{-6}F)*\ln 2=0.5 \text{ sec}$$

(7)In figure (4), the charging time t_2 after the second charging is calculated as follows:

$$t_2=R_A*C*\ln 2= (7.2x10^3\Omega)*(100x10^{-6}F)*\ln 2=0.5 \text{ sec}$$

(8)After the second charging, the output pulse of 555 astable multistage oscillator is shown as figure (5). In figure (5), except the transient state of first charging case, the whole period of pulse is T=1sec and the frequency is f= 1/T=1/1=1 (Hz)

(9)We can connect the pin of output voltage $V_3(t)[V_{out}]$ in figure (4) to the 14th pin of logic IC7490(a) in figure (1). Hence, this arrange shall transfer the IC7490(a) into a counter for a frequency divider of 10.

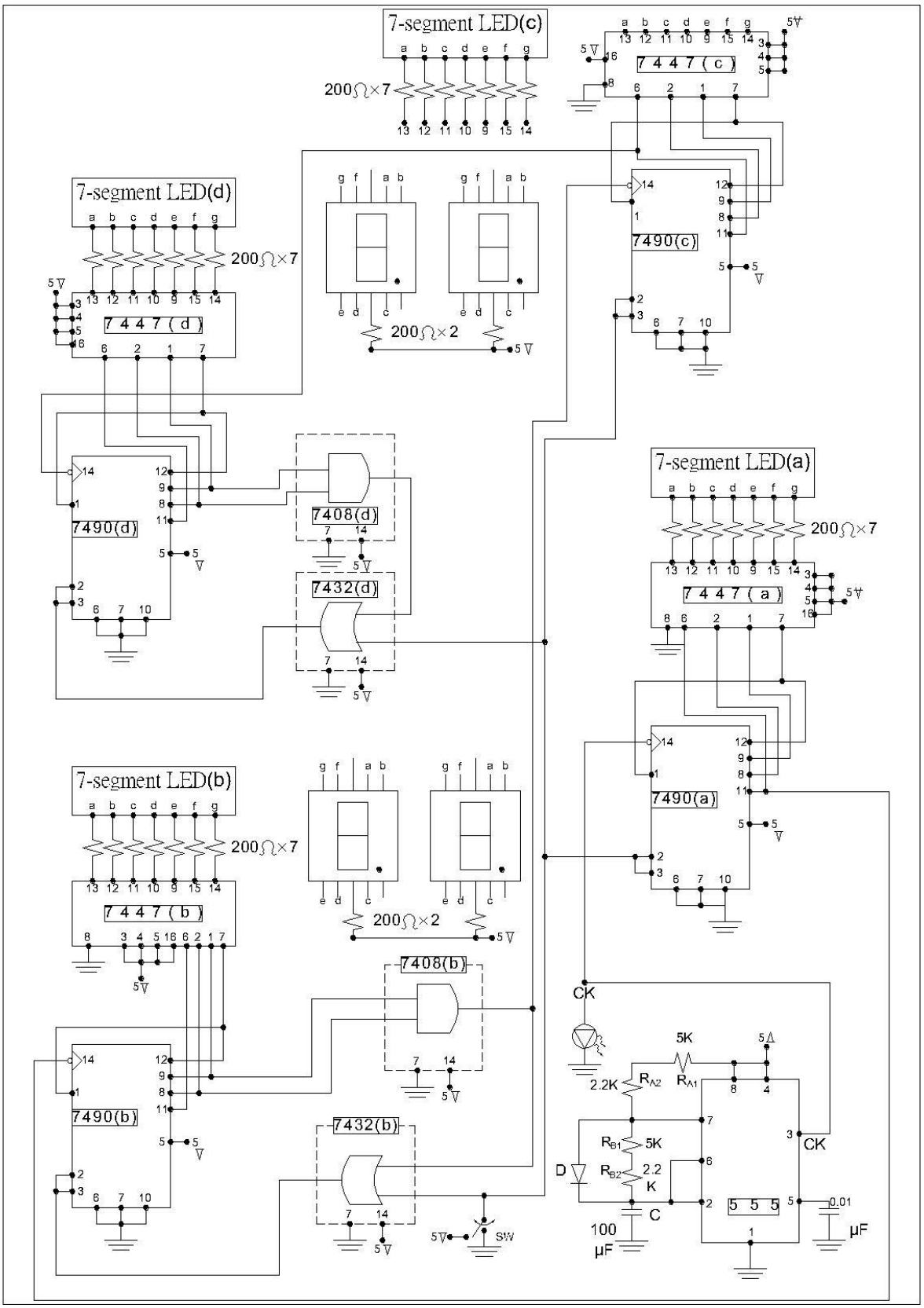


Fig.(1) global electric circuit diagram

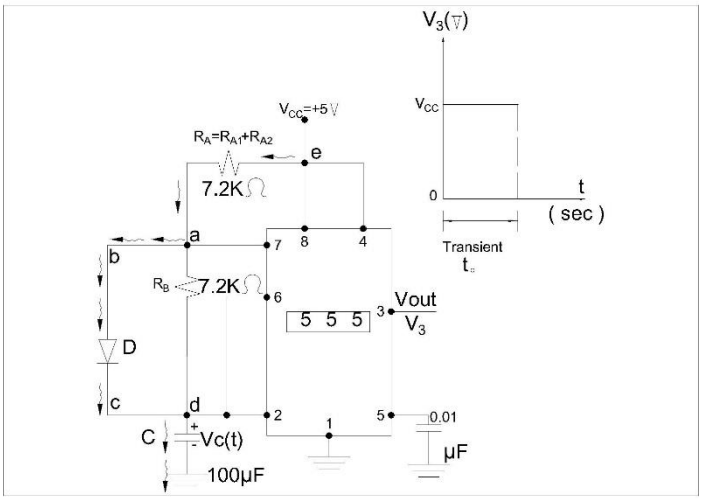


Fig.(2) the current path of the first charging

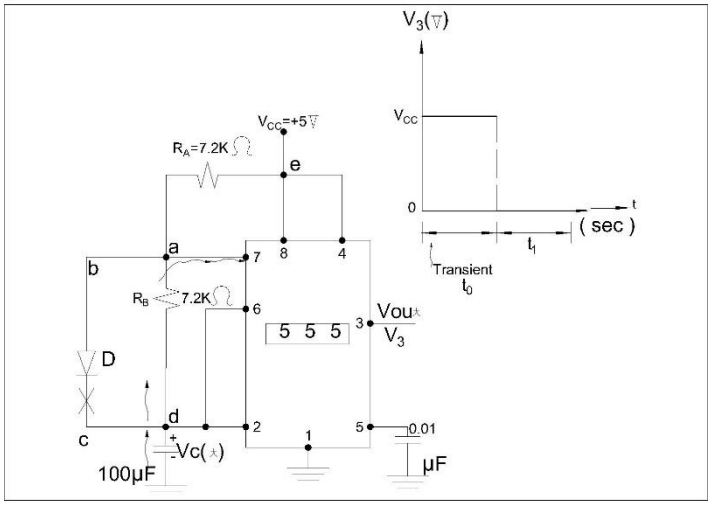


Fig.(3) the current path of discharging

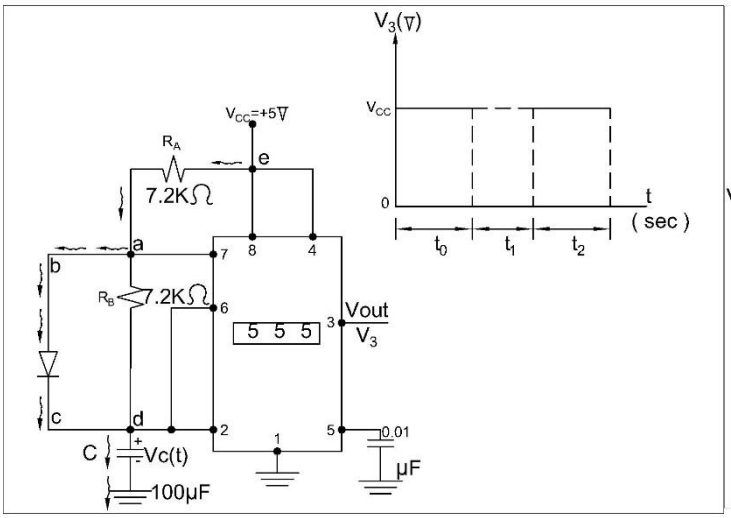


Fig.(4) the current path of the second charging

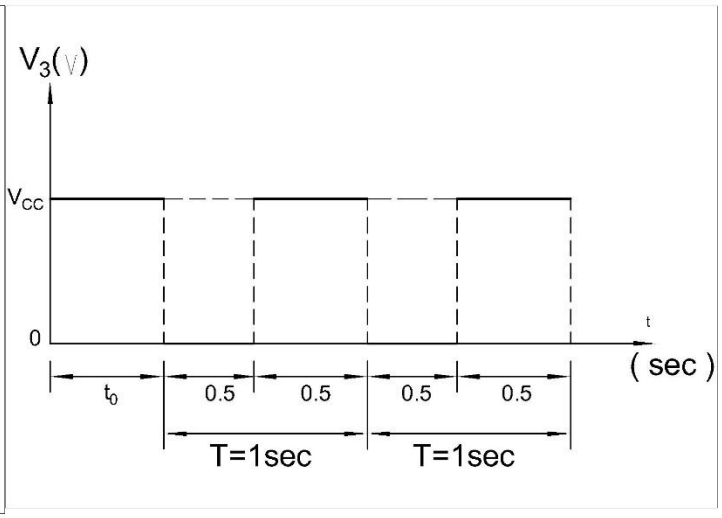


Fig.(5) the overall output pulse of 555 oscillator

IV. Detail Principle of Logic Circuit

(1) SW (switch) is the reset of counter in this research paper. When SW is set up to / (5V) (high potential), then, the counter is displayed to the start. The logic circuit is shown as figure (6). In spite of the digital pulse of 555 oscillator is sent to CK4 continuously, it cannot still stimulate the IC7490 (a), so there are no signal is sending to CK3, CK2 and CK1. The LED displayer is denoted as 00:00 all the time.

(2)When SW is set up to ϕ (0V) (grounded), the logic situation before the 3600th trigger of CK4 is shown as figure (7). The LED displayer is denoted as 59:59

(3)When SW is set up to ϕ (0V) (grounded), the logic situation of the first temporality after the 3600th trigger of CK4 is shown as figure (8). IC7490 (a) is returned to zero, that is, B3:/→ϕ, B0:/→ϕ. At the same temporality, according to B3:/→ϕ, it promotes CK3:/→ϕ (negative edge-triggered). The LED displayer is denoted as 59:50

(4) When SW is set up to ϕ (0V) (grounded), the logic situation of the second temporality after the 3600th trigger of CK4 is shown as figure (9). Because of CK3:/→ϕ (negative edge-triggered), it promotes the IC7490(c) carry-out, that is, B5:ϕ→/, B4:/→ϕ. The LED displayer is denoted as 59:60

(5)When SW is set up to ϕ (0V) (grounded), the logic situation of the third temporality after the 3600th trigger of CK4 is shown as figure (10). Because of the output of AND2 gate is / (high potential), it promotes the output of OR2 gate is / (high potential) and the input of CK2 is / (high potential). The incidental effect is that the IC7490 (b) is returned to zero. The LED displayer is denoted as 59:60

(6)When SW is set up to ϕ (0V) (grounded), the logic situation of the fourth temporality after the 3600th trigger of CK4 is shown as figure (11). Because the IC7490(b) is returned to zero, therefore B6:/→ϕ, B5:/→ϕ. The incidental effect is that the output of AND2 gate is transferred to ϕ(0V)(grounded) and CK2:/→ϕ (negative edge-triggered). The LED displayer is denoted as 59:00.

(7)When SW is set up to ϕ(0V) (grounded), the logic situation of the fifth temporality after the 3600th trigger of CK4 is shown as figure (12). Because CK2 is negative edge- triggered, therefore IC7490(c) is returned to zero (or reset) B11:/→ϕ, B8:/→ϕ. It promotes CK1:/→ϕ (negative edge-triggered).The LED displayer is denoted as 50:00

(8)When SW is set up to ϕ (0V) (grounded), the logic situation of the sixth temporality after the 3600th trigger of CK4 is shown as figure (13). Because CK1 is negative edge-triggered, therefore the IC7490 (d) can carry out, that is, B13:ϕ→/, B12:/→ϕ. The LED displayer is denoted as 60:00

(9)When SW is set up to ϕ (0V) (grounded), the logic situation of the seventh temporality after the 3600th trigger of CK4 is shown as figure (14). Because the output of AND1 gate is transferred to / (high potential), therefore the output of OR1 gate is transferred to / (high potential) and the IC7490(d) is returned to zero. The LED displayer is denoted as 60:00.

(10)When SW is set up to ϕ(0V) (grounded), the logic situation of the eighth temporality after the 3600th trigger of CK4 is shown as figure (15).Because the IC7490(d) is returned to zero, therefore B14: /→ϕ, B13: /→ϕ. The LED displayer is denoted as 00:00

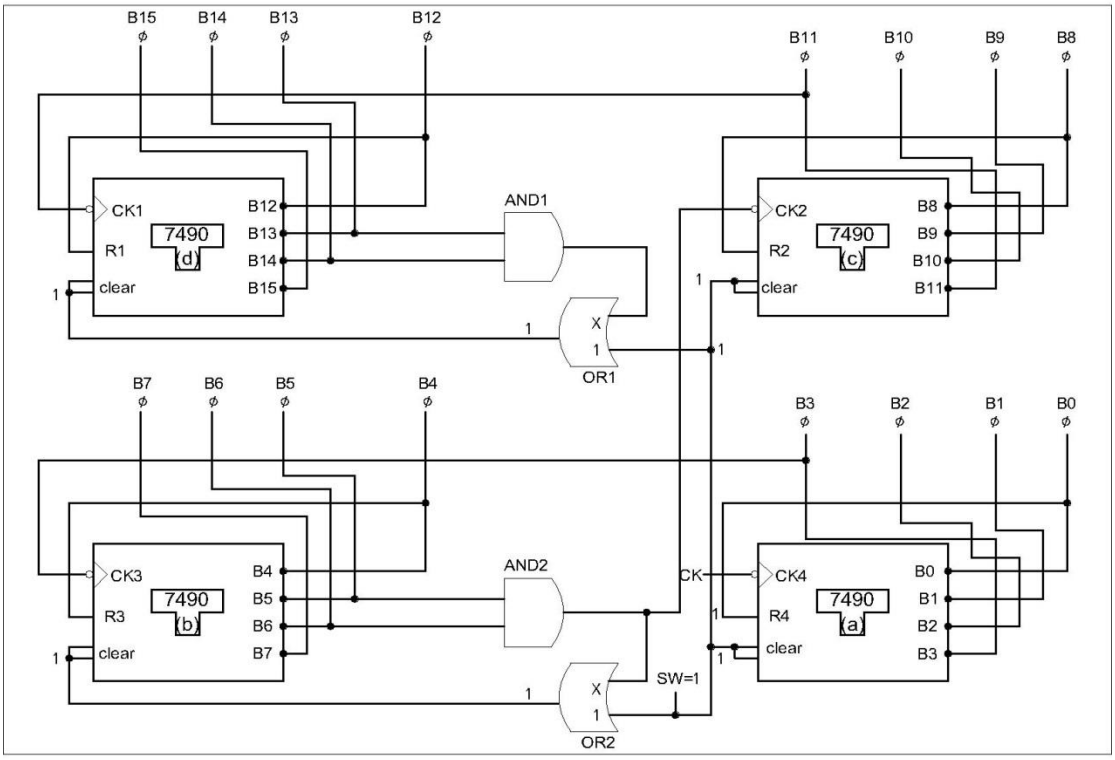


Fig.(6) the logic diagram for the case of SW=1(5V)

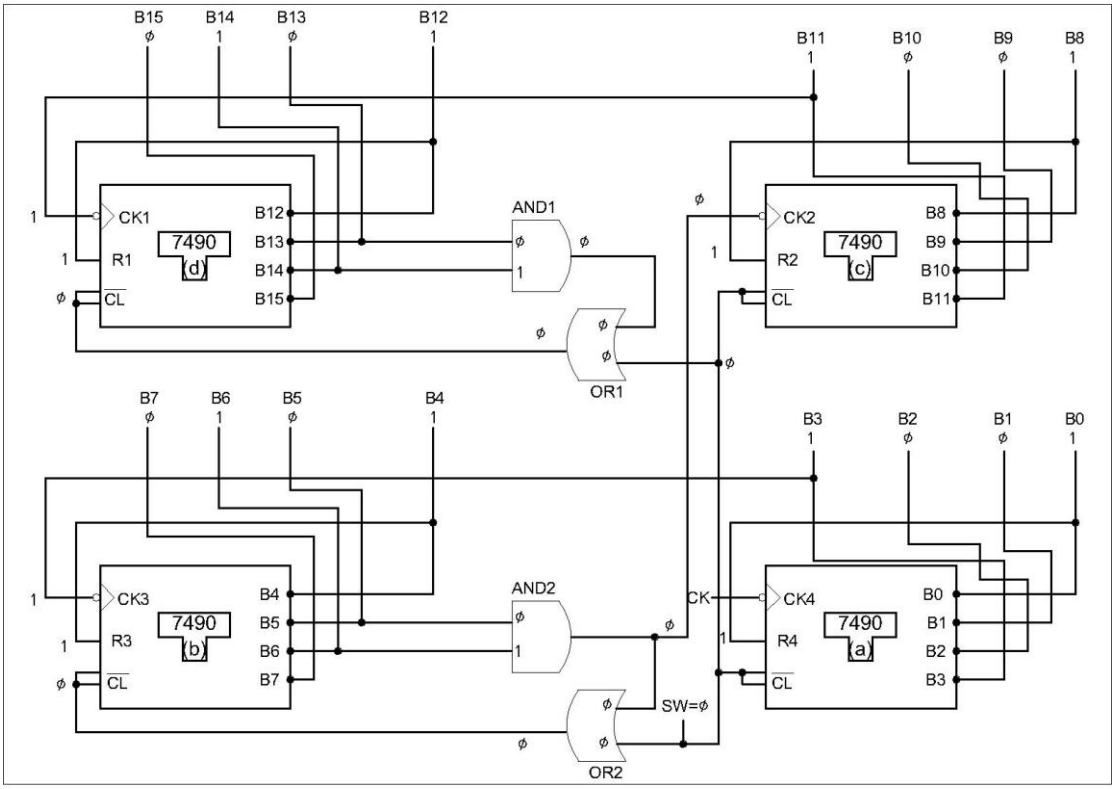


Fig.(7) the logic state before the 3600th trigger at CK4

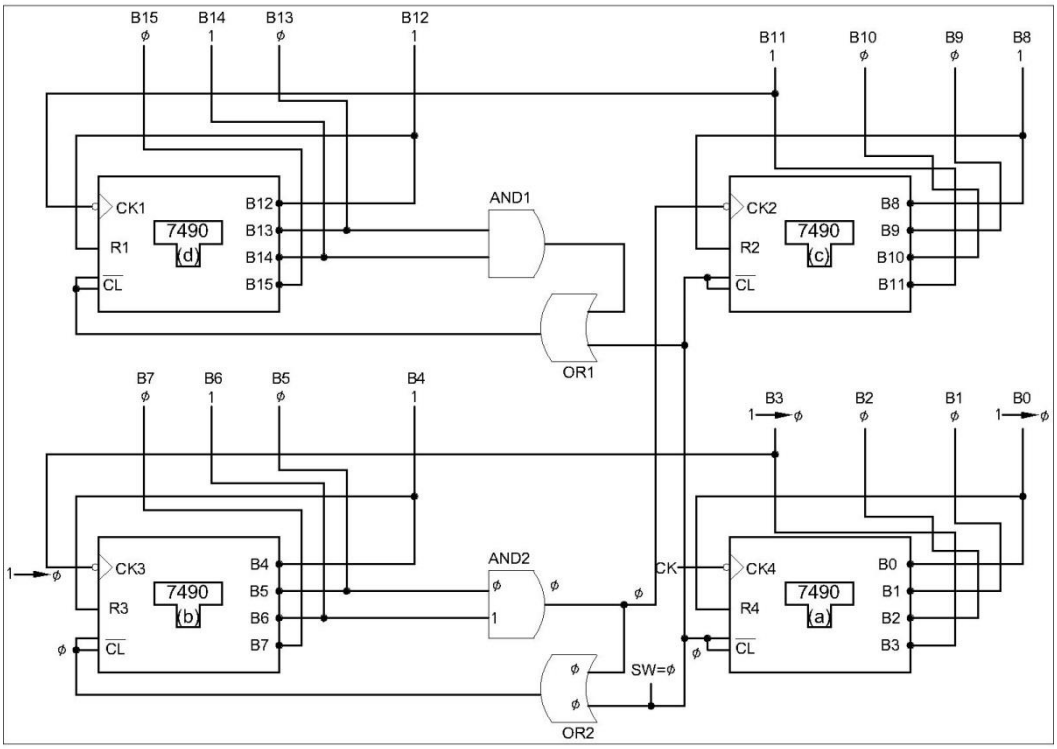


Fig.(8) the first temporality after the 3600th trigger at CK4

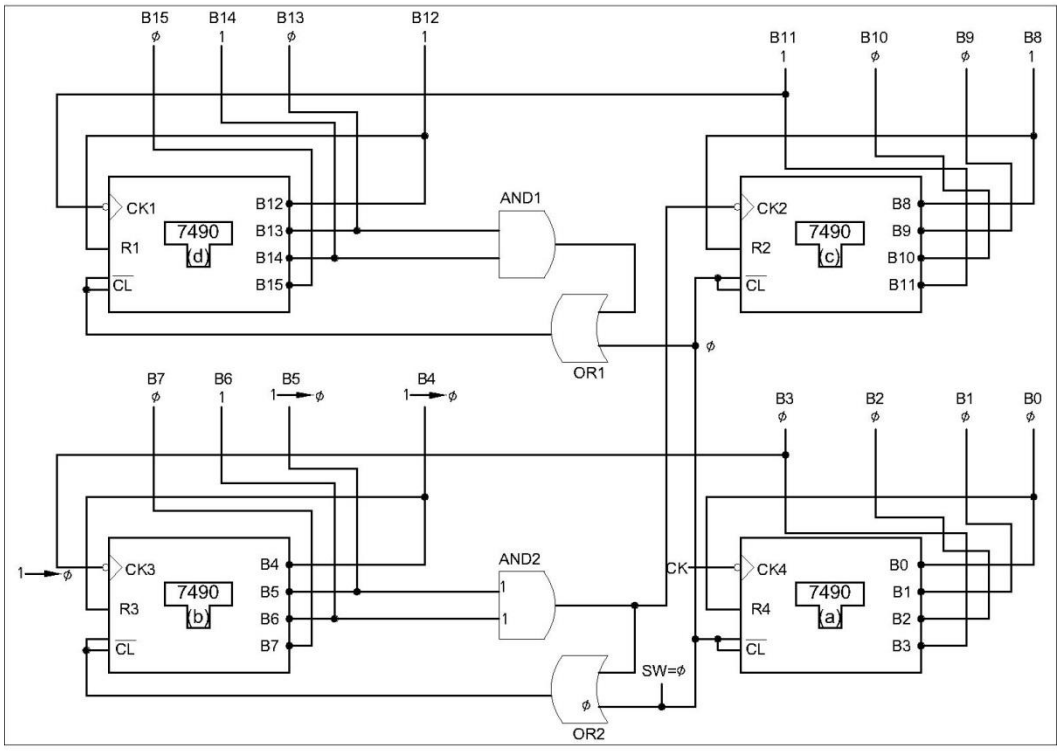
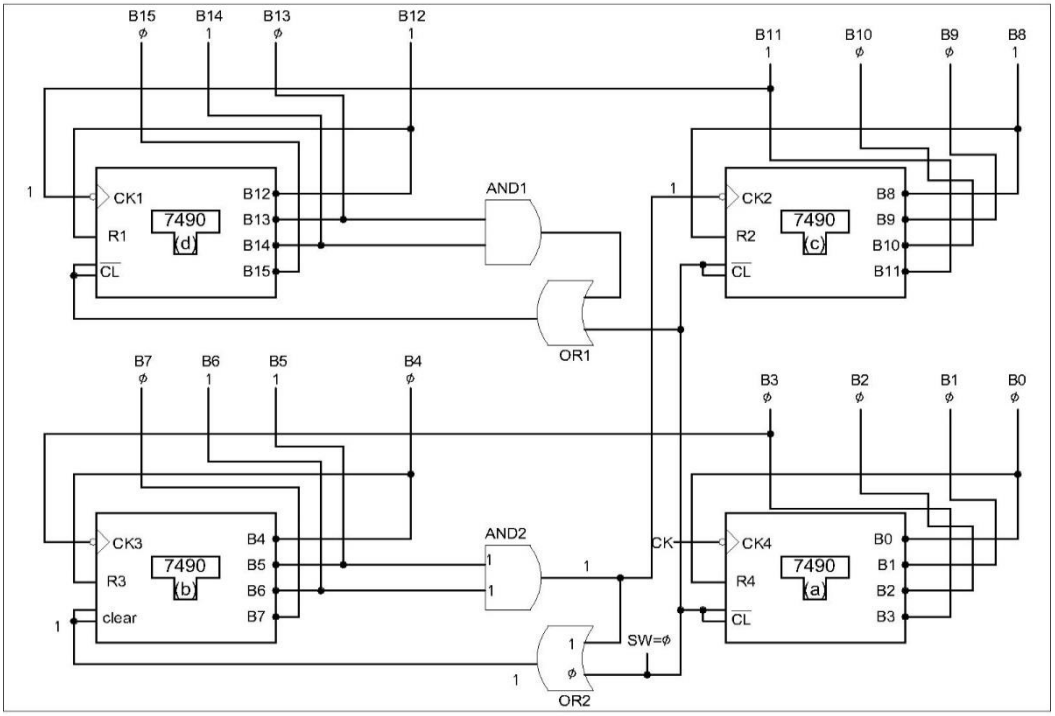


Fig.(9) the second temporality after the 3600th trigger at CK4



Fig,(10) the third temporality after the 3600th trigger at CK4

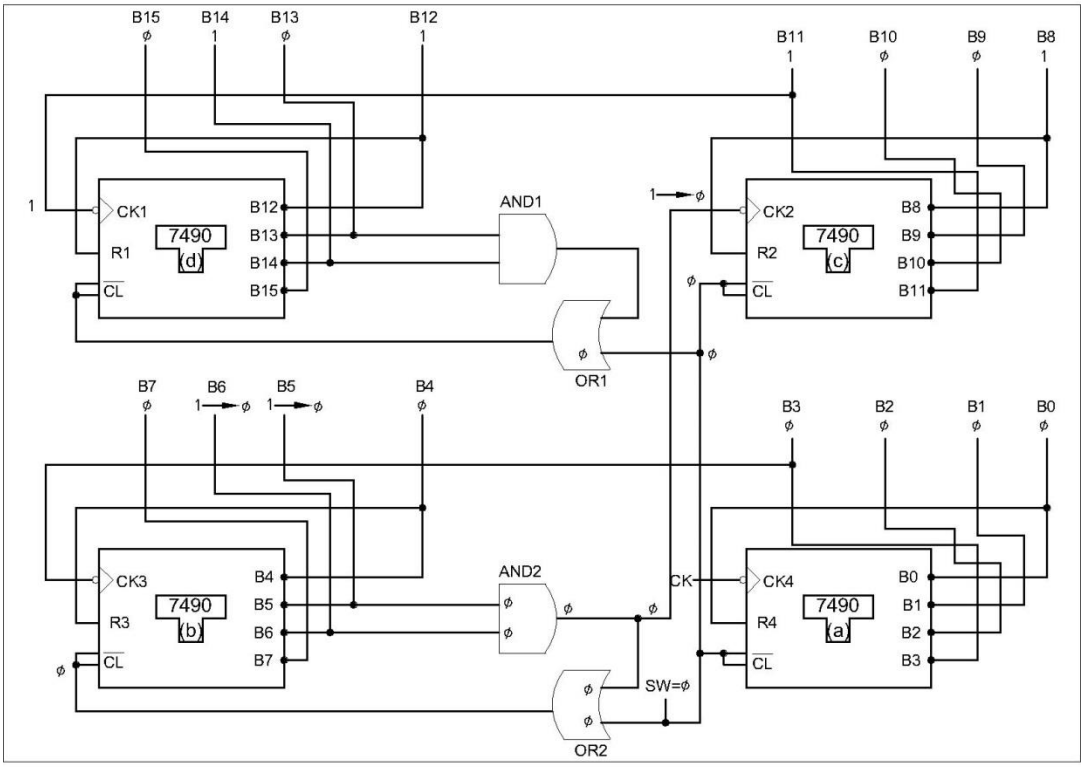


Fig.(11) the fourth temporality after the 3600th trigger at CK4

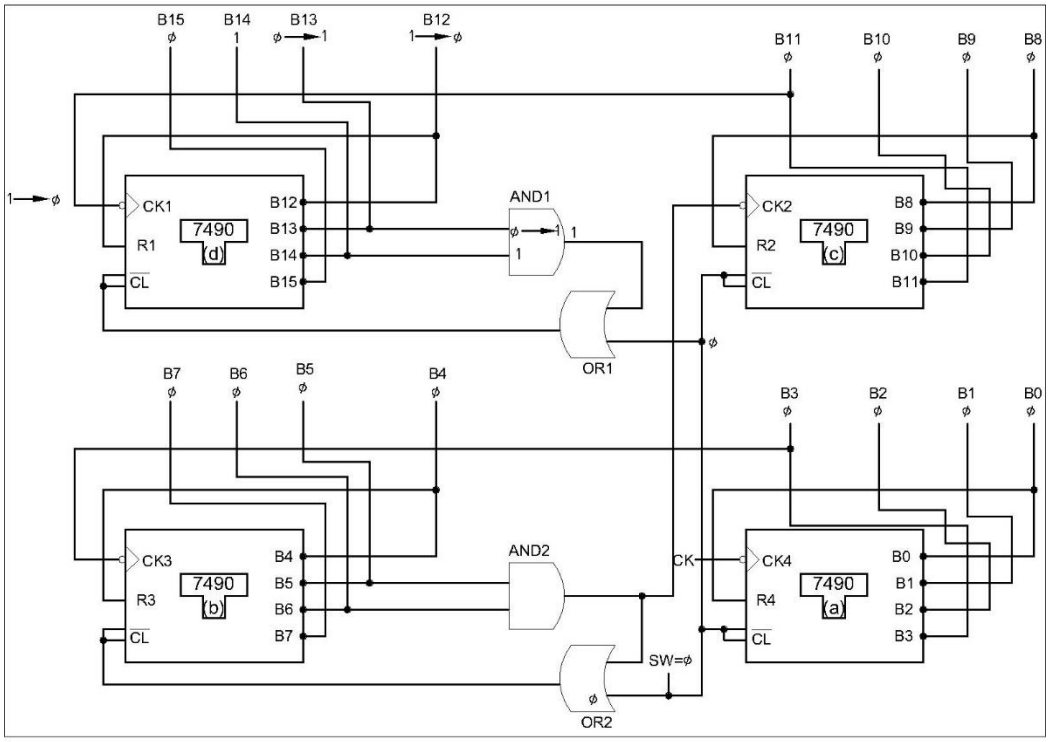


Fig.(12) the fifth temporality after the 3600th trigger at CK4

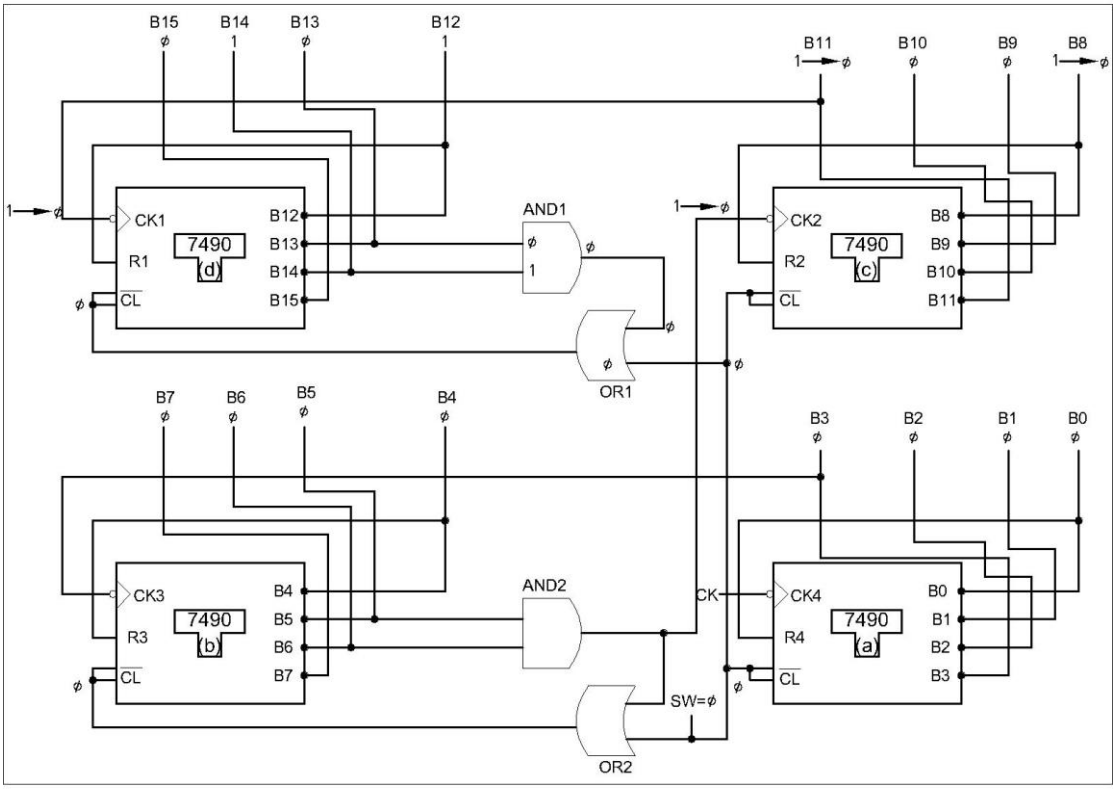


Fig.(13) the sixth temporality after the 3600th trigger at CK4

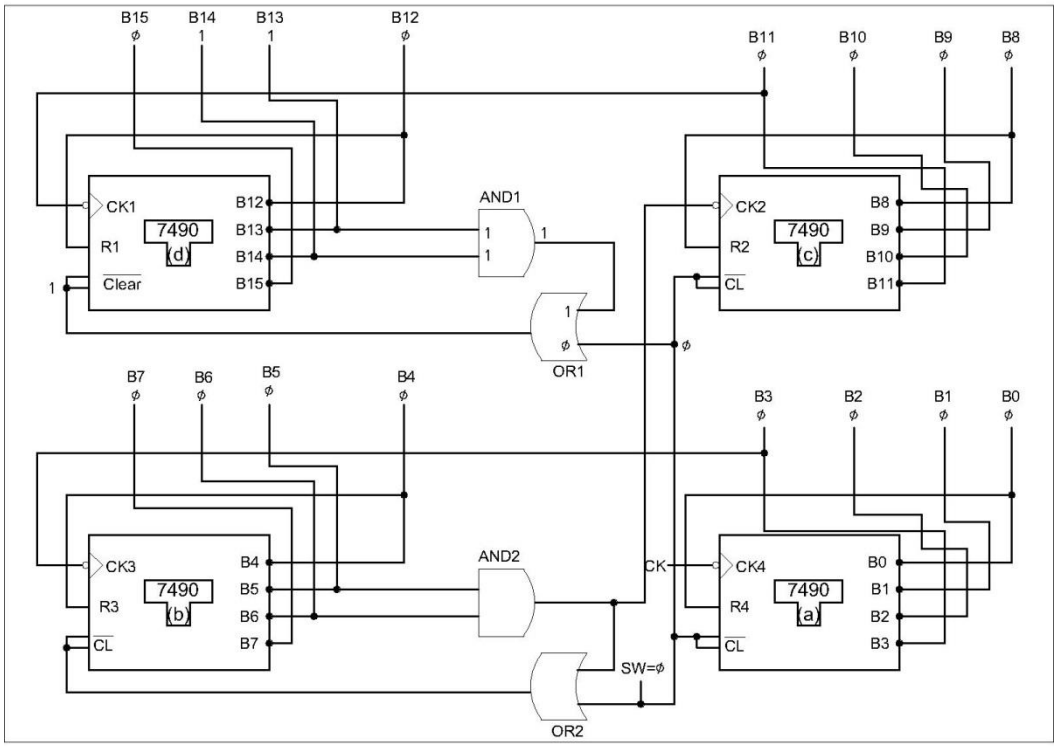


Fig.(14) the seventh temporality after the 3600th trigger at CK4

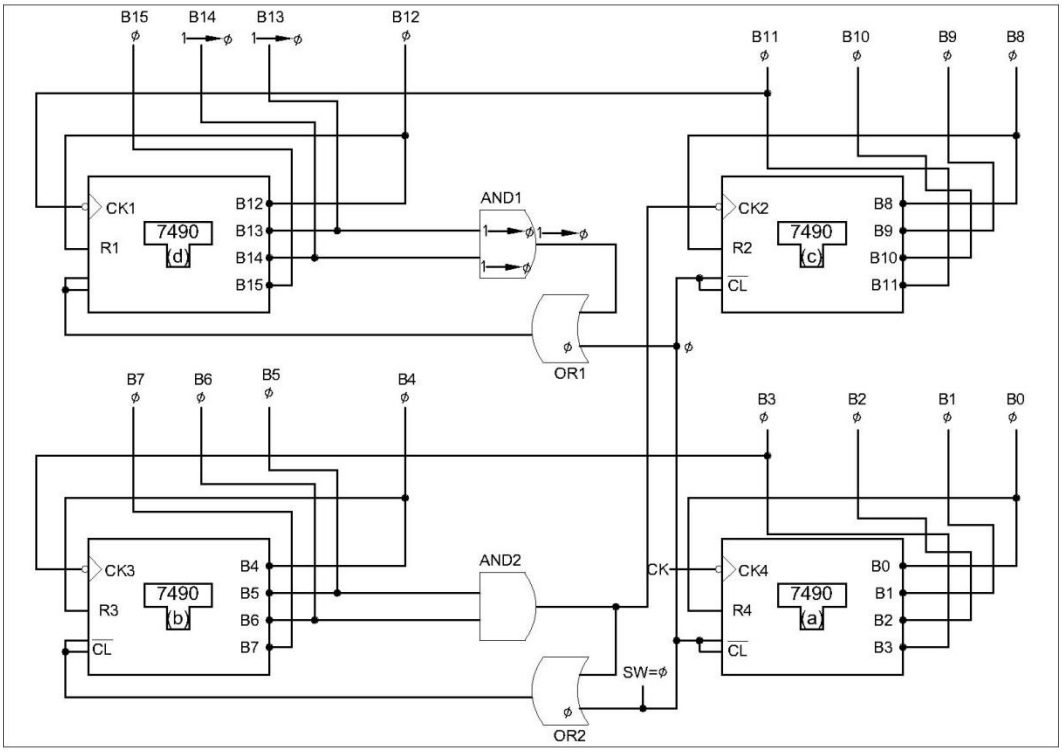


Fig.(15) the eighth temporality after the 3600th trigger at CK4

V. Experiment results (The truth table)

CK	SW	minutes									seconds								
		B15	B14	B13	B12	B11	B10	B9	B8	Display	B7	B6	B5	B4	B3	B2	B1	B0	Display
×	1	×	×	×	×	×	×	×	×	00	×	×	×	×	×	×	×	×	00
1	ø	ø	ø	ø	ø	ø	ø	ø	ø	00	ø	ø	ø	ø	ø	ø	ø	1	01
2	ø	ø	ø	ø	ø	ø	ø	ø	ø	00	ø	ø	ø	ø	ø	ø	1	ø	02
3	ø	ø	ø	ø	ø	ø	ø	ø	ø	00	ø	ø	ø	ø	ø	ø	1	1	03
⋮	ø	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
3599	ø	ø	1	ø	1	1	ø	ø	1	59	ø	1	ø	1	1	ø	ø	1	59
3600	ø	ø	ø	ø	ø	ø	ø	ø	ø	00	ø	ø	ø	ø	ø	ø	ø	ø	00

Fig.(16) truth table (symbol ”x” denote don’t care)

VI. All completed photo.

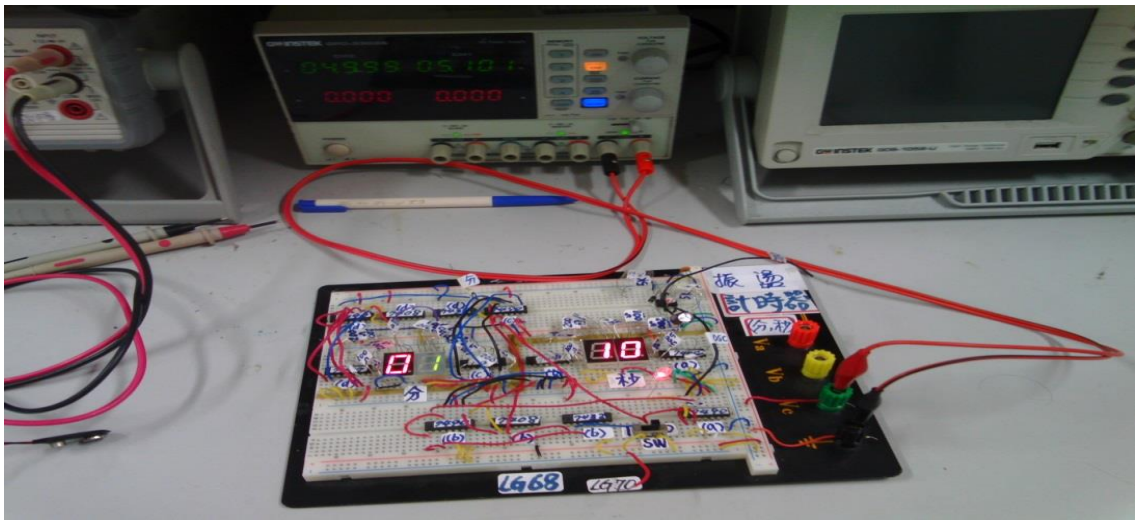


Fig.(17) all completed photo.

VII. Conclusion

(1)The output pulse of astable multistage oscillator in the first part of this research paper is transient state only as shown in figure (2). The required time t_0 is difficult to estimate so that we don't study it in depth. After the first discharging (the required time is t_1 (seconds)) and the second charging (the required time is t_2 (seconds)), the output pulse is steady state as shown in figure (5), therefore we define the astable multistage oscillator as the source of digital pulse shown as figure (5).

(2)We design the $R_{A1}+R_{A2}=7.2k\Omega$ and the capacitance C=100μF on purpose under the charging process of 555 oscillator in this research paper so that we can adjust the required time of charging process to $t_2=0.5$ sec. Similarly, in order to adjust the discharging time to $t_1 = 0.5$ sec, we can adjust $R_B = R_{B1} + R_{B2}=7.2k\Omega$ and the capacitance C = 100μF. Under this case, the total period $T=t_1+t_2= 0.5+ 0.5=1$ sec, the duty cycle= $(t_1/T) * 100\% = (0.5 / 1)*100\%=50\%$ and the frequency f=1/T=1/1=1(Hz)

(3)The performance of IC7408 (AND gate) in this research paper is to make MOD-60. When the second number has reached to 60, it can take one minute. When the minute number has reached to 60, it can totally return to zero

(4)The performance of IC7432 (OR gate) is to perform cleaning in this research paper. When SW=/ (high potential), we can do the cleaning over the total IC7490. When the output of IC7408 is / (high potential), we can do the cleaning over the ten digits of minute and second.

(5)In order to avoid any confusion, we identify the IC number such as (a) (b) (c) (d) after the logic IC.

(6) If a mode 24 oscillation counter with a frequency of f=1Hz is added to the back end of this paper, a clock can be formed.

(7) The biggest feature of this paper is "to replace the traditional function generator with 555 astable multistage oscillator". This approach can greatly simplify the structure of this paper and reduce errors so that it can enter the feasibility assessment of commercial use (commercialization).

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