Journal of Multidisciplinary Engineering Science and Technology (JMEST)
ISSN: 2458-9403
Vol. 5 Issue 10, October - 2018

Digital Demultiplexer (1x8)

Shih-Ping Hu
Department of mechanical engineering
Hungkuo Delin University of Technology
New Taipei City, Taiwan, Republic of China
hushihping@yahoo.com.tw

***Abstract*—With the advancement of human science and technology, the digitalization of electromechanical products is an inevitable trend, for example; computers, mobile phones, digital TVs, digital remote control refrigerators, satellite navigation systems and even military weapons, etc., are numerous. This paper is for the channel system of cable television. Channel operators produce a variety of different entertainments and news programs that are aggregated through a multiplexer on a single wire and transmitted to a consumer's digital TV. Consumers have a demultiplexer in the television set and they can choose the appropriate channel to watch the program according to their personal interests.**

Keywords—electromechanical products, satellite navigation systems multiplexer, demultiplexer, mobile phones

I. Introduction

This paper is to design a simplest demultiplexer with the lowest cost. The meaning of "1X8" is that an input signal I can be transmitted to a specified output address Y with different binary selection ($S_2S_1S_0$)(the output address has eight addresses)

II. Literature review

We will give some examples in

the research field of demultiplexers in previous years. In the literature [1], Guo Mingshan graduate student studied the research and comparison of the demultiplexer and decoder in the player in his master's thesis, specially the difference between the decoder and the demultiplexer. In the literature [2], Huang Zhuyu graduated student studied the integration of long-wavelength plastics and optical multiplexers and demultiplexers in his master's thesis, specially the performance difference between optical multiplexer and demultiplexer.

III. Principle explanation

(1) Electronic components that we use in this research paper have ①logic IC 74LS04*1, 74LS47*1, 74LS21 *4 ②3 point 2 paragraph sliding switch*3 ③ resistance 2.2KΩ*3, 330Ω*7, 200Ω*8 ④LED light*8 ⑤ common anode seven-segment LED monitor (small type)*1 ⑥circuit strip*1

(2)The design of the logic IC7404 is completely reversed, and its detailed structure is shown in figure (1).

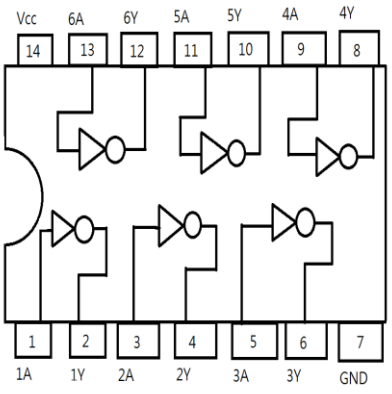

Fig.(1) the original construction digaram of IC7404

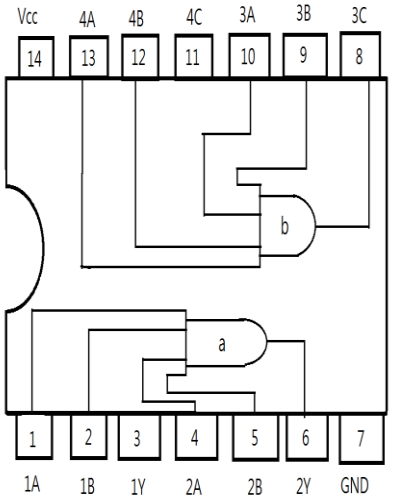

Fig.(2) the original construction diagram of IC 7421

(3)The design of logic IC7421 is completely the function of AND gate. Each IC7421 is equipped with two sets of AND gates as shown in figure (2). According to the characteristics of the AND gate, all four inputs must be high potential “/” to have a high potential output “/”.

IV. The overall circuit wiring diagram

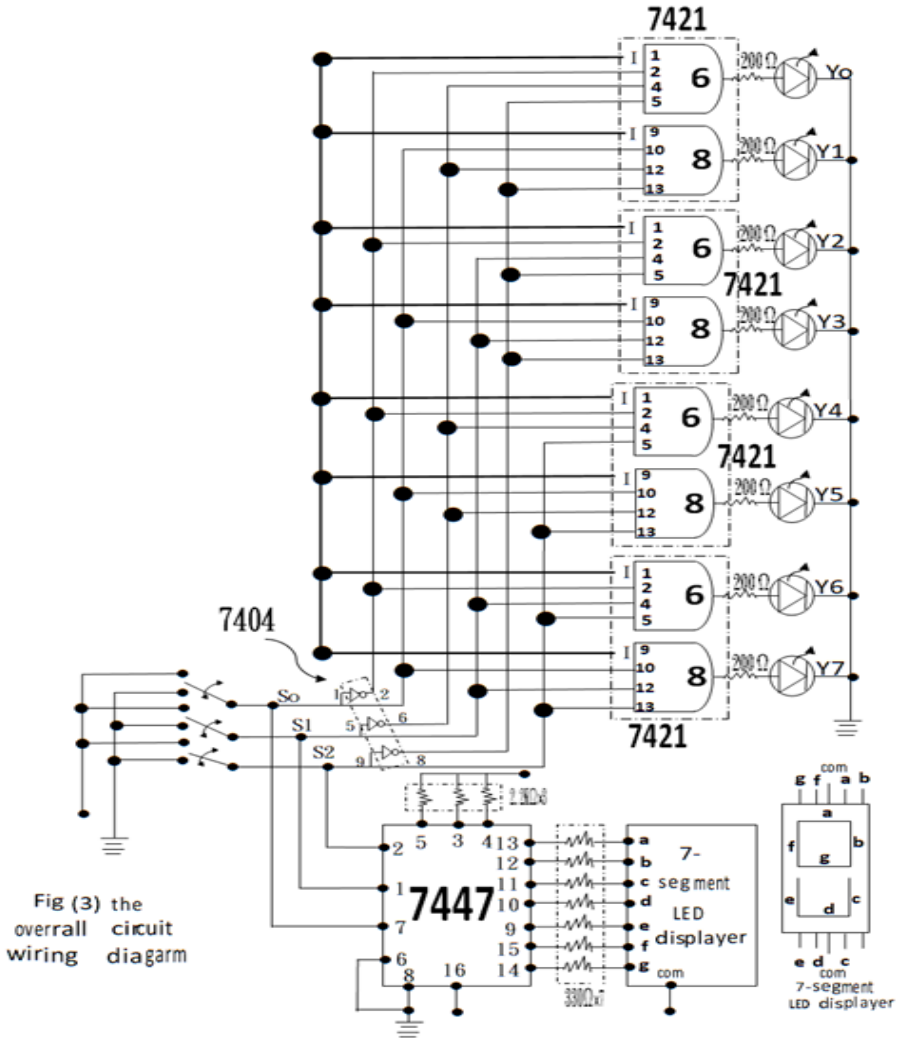

Fig (3) the overrall circuit wiring diagarm

V.The detail principle of individual components

(1) Logic IC7404 is the role of the reverse gate. When S_0 inputs the high potential signal "/". Then, this signal enters from pin 1 of IC7404 at the same time. When the signal is output from pin 2 of IC7404. Then, it has become low potential "Ø" as shown in figure (4).

(2) When S_0 input the low potential signal "Ø". Then, this signal enters from pin 1of IC7404 at the same time. When the signal is output from pin 2 of IC7404. Then, it has become high potential "/" as shown in figure (5).

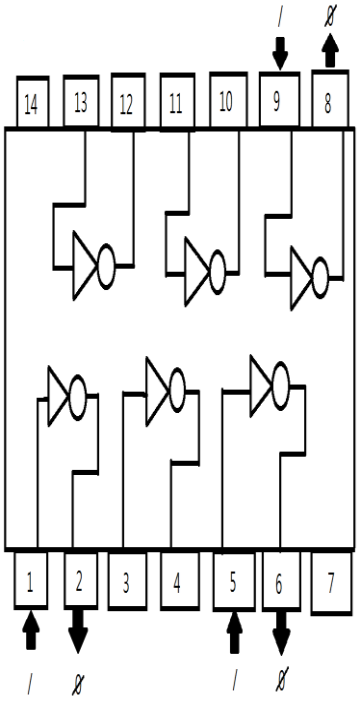

Fig.(4) the case of S2 S1 S0 all inPut high potential"/"

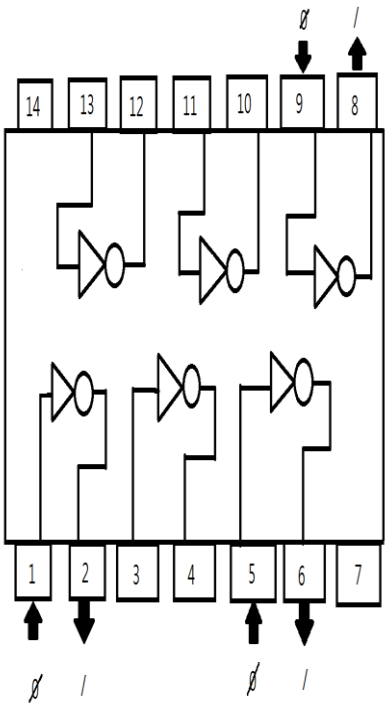

Fig.(5) the case of S2 S1 S0 all input low potential"Ø"

(3) Similarly, it can be known that when S_1 inputs the high potential signal "/". Then, this signal enters pin 5 of IC7404 at the same time. When the signal is output from pin 6 of IC7404. Then, it has become low potential "Ø" as shown in figure (4).

(4) When S_1 input the low potential signal "Ø". Then, this signal enters from pin 5 of IC7404 at the same time. When the signal is output from pin 6 of IC7404. Then, it has become high potential "/" as shown in figure (5).

(5) IC7421 is the function of AND gate. When input pins are all high potential "/". Then, the output pin will be high potential "/" as shown in figure (6).

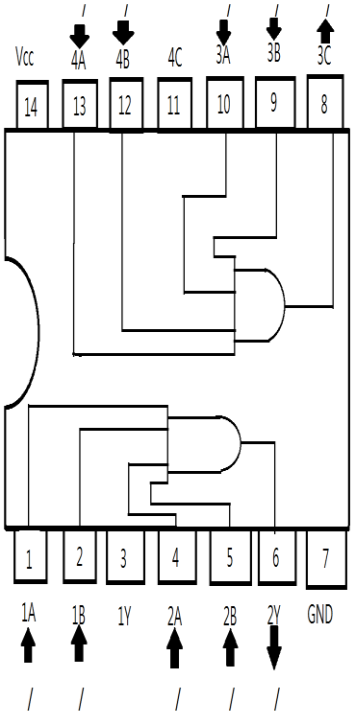

Fig.(6)IC7421 input high potential"/"

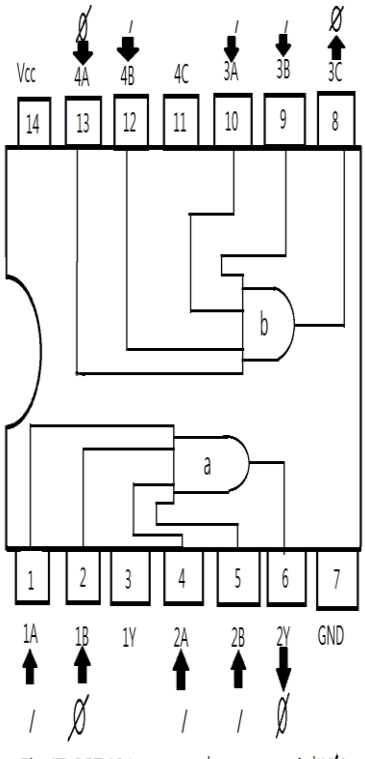

Fig.(7) IC7421 out put low potential"Ø"

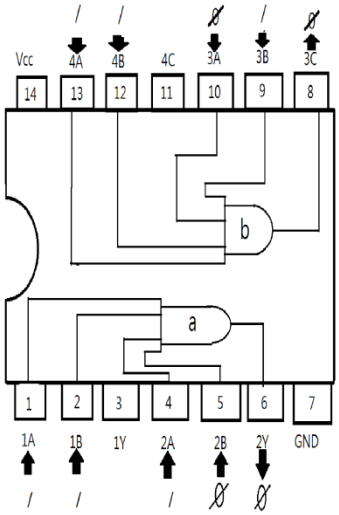

Fig.(8) IC7421 output low potential"Ø"

(6) In figure(7), for the NAND gate(a); although the input of pins 1, 4 and 5 are all high potential "/", the output of pin 6 is caused to low potential "Ø" by the input of pin 2 being low potential "Ø". For the NAND gate(b); although the input of pins 9, 10 and 12 are all high potential "/", the output of pin 8 is caused to low potential "Ø" by the input of pin 13 being low potential "Ø".

(7) In figure(8), for the NAND gate(a); although the input of pins 1, 2 and 4 are all high potential "/", the output of pin 6 is caused to low potential "Ø" by the input of pin 5 being low potential "Ø". For the NAND gate(b); although the input of pins 9, 12 and 13 are all high potential "/", the output of pin 8 is caused to low potential "Ø" by the input of pin 10 being low potential "Ø".

(8) In figure(3), paralleling the input command $S_2S_1S_0$ to IC7447 is to convert the input command to a different low-potential command (0 V) to drive the common anode seven-segment displayer.

(9) The structure of the common anode seven-segment LED display is shown in figure (9)

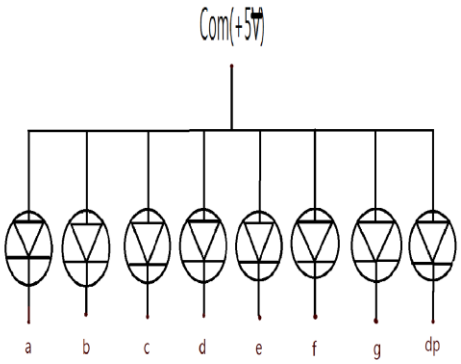

Fig.(9) the internal structure of common anode 7-segment LED displayer

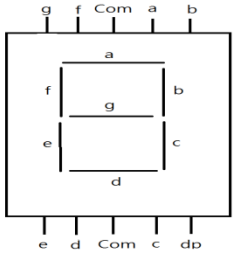

Fig.(10) the corresponding pin diagram of 7-segment LED dusplayer

(10)It is known in figure (9); when the a, b, c, d, e, f, g pins are low potential "Ø". Then, the corresponding LED lights will be on.

(11)For example: When the command $S_2S_1S_0$=Ø//$_{(2)}$=3$_{(10)}$ is entered; then, the 2,1 and 7 pins of IC7447 have a low potential of "Ø", a high potential of "/", and a high potential of "/" respectively. The output of pins 13,12,11,10,14 of IC7447 are low potentials "Ø", the output of pins 9, 15 of IC7447 are high potentials "/"; then, the seven-segment display a= b=c=d=g="Ø" (low potential), f=e ="/"(high potential), the number on the display is "3", as shown in figure (11).

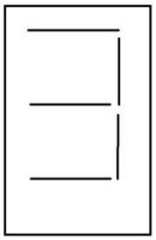

Fig .(11) the display map when a= b=c=d=Ø (low potenwial)

VI. Principle of logic circuit

(1) Let the input command (selection) is $S_2S_1S_0$=Ø//$_{(2)}$=3$_{(10)}$, the logic circuit can be obtained as shown in figure(12). Then, you can get Y_3="/ " and the rest are zero (Y_0=Y_1=Y_2 = Y_4=Y_5= Y_6=Y_7 ="Ø")

(2) Let the input command (selection) is $S_2S_1S_0$=//Ø$_{(2)}$=6$_{(10)}$, the logic circuit can be obtained as shown in figure(13). Then, you can get Y_6=/ and the rest are zero (Y_0=Y_1=Y_2 = Y_3=Y_4=Y_5=Y_7=Ø)

(3) Using a simple schematic diagram, the "Demultiplexer (1X8)" is shown in figure (14).

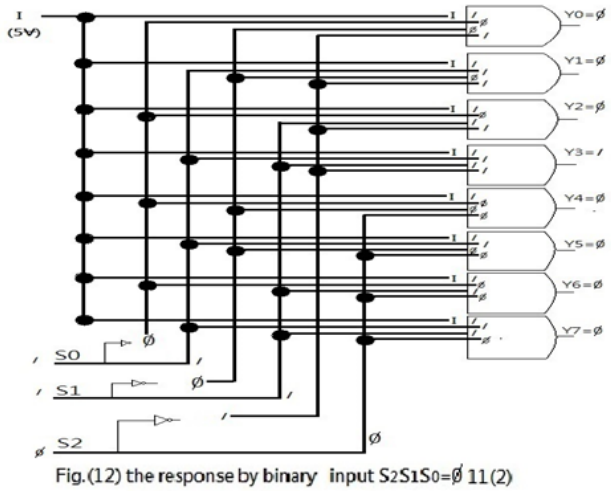

Fig.(12) the response by binary input $S_2S_1S_0$=Ø 11(2)

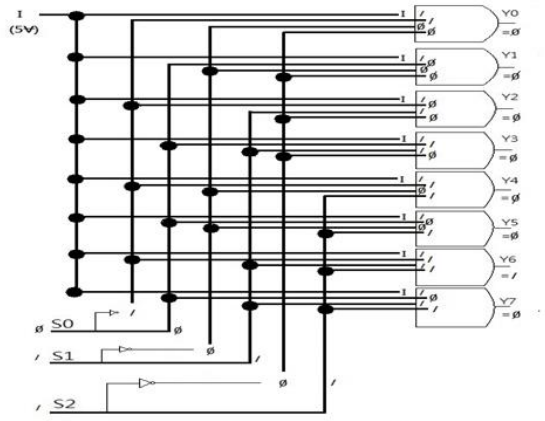

Fig.(13) the response by binary input S2S1S0=11Ø(2)

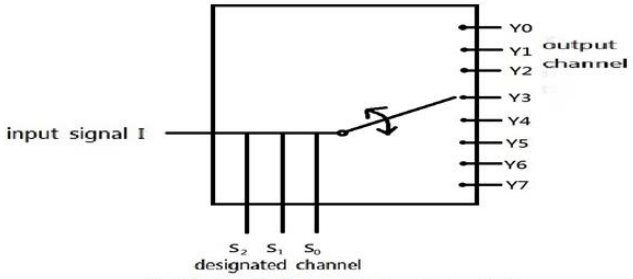

Fig.(14)schematic diagram of the demultiplexer(1x8)

VII. Completed photo of the demultiplexer(1X8)

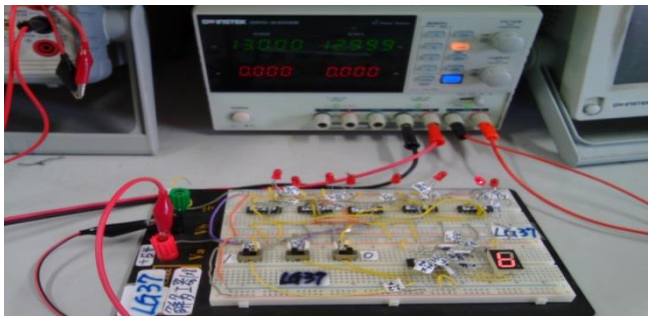

Photo.(1)

VIII.Experiment result (the truth table)

input signal I	S_2	S_1	S_0	displayer	bright LED
I=1(5V)	Ø	Ø	Ø	0	Y0
	Ø	Ø	/	1	Y1
	Ø	/	Ø	2	Y2
	Ø	/	/	3	Y3
	/	Ø	Ø	4	Y4
	/	Ø	/	5	Y5
	/	/	Ø	6	Y6
	/	/	/	7	Y7

Fig.(15) the truth table

IX. Conclusion

(1) Because the input command $S_2S_1S_{0\,(2)}$ is a 3-bit binary number plus the input signal I(5V) becomes 4 bits in total, resulting in 4 inputs for each AND gate . Then, IC7421 is used in this paper.

(2) The three 2.2KΩ resistors in figure (3) are designed to protect the logicIC7447 from the DC voltage source(5V) input too strong current and damage the logic IC7447.

X. Reference

[1]Guo Mingshan graduate student (1997) "*research and comparison of the demultiplexer and decoder in the player"*, master's thesis; Hsinchu, Taiwan; national Chiao- Tung university, Department of Telecommunication Engineering.

[2]Huang Zhuyu graduated student (1992) "*the integration of long- wavelength plastic optical fiber and optical multiplexers and demultiplexers"*, master's thesis; Taoyuan, Taiwan; Chang Gung university, Department of Optoelectronic Engineering.

[3](2001), "*Exchange table of the specification between TTL/IC in the world"*, (page 58, 84, 116), Taiwan; Chuan Hwa book Co. LTD.

[4]Chang Zianan (2008), "*Digital logic design laboratory"*, Book Co. LTD of Taiwan science and Technology, page 167~171, 154~162, first edition, Taiwan, March