

Design and Simulation of Balanced RF Power Amplifier over Adaptive Digital Pre-distortion for MISO WLAN-OFDM Applications

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Abstract—This paper presents a design and simulation of energy efficient power amplifier for Multiple-Input-Single-Output (MISO) Wireless Local Area Network (WLAN) Orthogonal Frequency Division Multiplexing (OFDM) applications, operating with lateral MOSFET transistor device between 2.620 to 2.690 GHz frequency bands. The power added efficiency reach up to 52 percent at 41dBm p_{out} . The amplitude and phase modulation coefficients are extracted from single tone test. However, new model has been proposed to extend Saleh model, in which the polynomials are modelled using adaptive digital pre-distortion system in WLAN-OFDM IEEE 802.11a physical layer transmitter. The performance of the adaptive digital pre-distorter using the modified Saleh model characterize and compensate the effect of nonlinearity of the power amplifier. This technique is considered useful in improving performance for the mobile communication applications.

Keywords—balanced power amplifier; multiple input single output; orthogonal frequency division multiplex; adaptive digital pre-distortion.

I. INTRODUCTION

The greatest challenge facing RF power amplifier devices in wireless communication systems is lack of persistent linearity in the presence of high efficiency. Power amplifier is the most energy consuming device in the transmission system, which more than 52% of the power is converted to a wasted heat energy. This condition progressively affects other devices in the transmitter and however, results to system performance reduction. A technique needs to be employed for dynamic amplification. The technique is to counter balance the cost of energy consumption from base station and improve long battery life of the mobile equipment [1].

Adaptive digital pre-distortion can be one of the most commonly used linearization technique. It is simple to apply and one of the most cost effective. Like other pre-distortion systems, adaptive pre-distortion use inverse parameters to characterize and compensate the nonlinearity and the memory effects of nonlinear power amplifier. The effect of harmonic

components and intermodulation distortion in power amplifier is a foremost apprehension for communication systems engineering [1]. The effects result to apparent presence of nonlinearity on the frequency band. These however, lead to power loss and adjacent channel interference. To mitigate these effects of nonlinearity and achieve state of the art system, it is obligatory to prudently design and implement the power amplifier for high speed data rate and spectral efficiency. A healthier power amplifier design is an exceptional candidate for technologies such as multiple-input-multiple-output (MIMO), wireless land area network (WLAN), orthogonal frequency division multiplexing (OFDM), spatial modulation transmitters and several more 5G applications. The features of such systems embrace high speed data rate, wider bandwidth and higher spectral efficiency [2, 3].

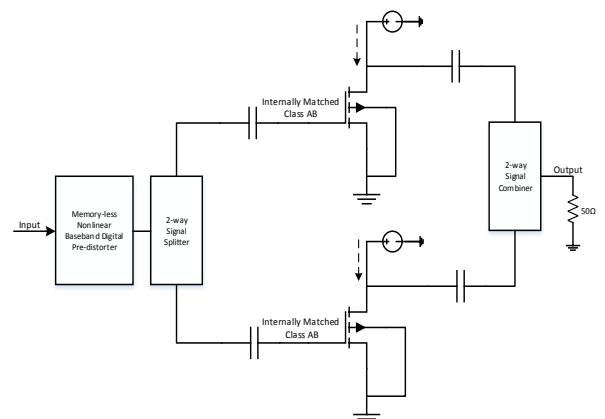


Fig. 1. Balanced power amplifier architecture with adaptive digital pre-distortion at the baseband.

This paper presents a discussion on the design of balanced RF power amplifier, the effect of nonlinearity and impact of adaptive digital pre-distorter in transmission system. Section II presents balanced power amplifier circuit design and performance results. Section III discusses adapting modified Saleh model for adaptive digital pre-distortion. Section IV presents conclusion of the paper.

II. BALANCED POWER AMPLIFIER CIRCUIT DESIGN AND PERFORMANCE RESULTS

The balanced power amplifier was designed using an Agilent advanced design system (ADS) software

with a free-scale n-channel enhancement mode lateral MOSFET MRF826060HSR3 transistor model, 2.620GHz to 2.690GHz frequency band. Figure 1 has shown 2 a cascaded class-AB power amplifiers. These circuit represent two amplifiers with gate source voltage to make it a balanced linear system. The two power amplifiers are connected together via a splitter at the baseband and a combiner at the output. The splitter at the baseband splits the signal into two at 90° phase shift to feed the amplifiers. The combiner at the output, combines the signal from the two transistors at 90° un-phase shift. A full wave signal is produced at the output [3].

In the design of balanced power amplifier, there are significant stages of design that are expected to observe:

A. Design of DC and Bias Circuits

DC circuit design can be done using Agilent advanced design system simulator. The DC simulation circuit is designed to define bias point and bias network. This is require in order to select the amplifier class of operation and power to be consumed by the device. The drain source voltage (VDS) is set to 28 volts, while the gate source voltage (VGS) is 2.4 volts respectively. This means that the bias condition has been set at the voltage source. However, these values have been recommended in the data sheet by the manufacturer. The design was simulated and drain source current (IDS) was achieved at 45mA as shown in figure 2. The DC quiescent current was achieved to prevent signal distortion [4, 5].

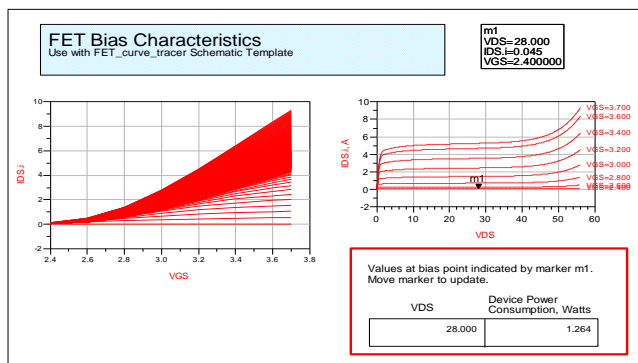


Fig. 2. DC IV curve simulation result.

Like the main purpose of DC simulation is to specify the class of operation and the DC quiescent current is to prevent signal distortion. Bias circuit was also designed based on class-AB carrier. A good biasing prevents signal reflection and distortions. In addition to setting the bias network component values, linecalc from ADS simulator is to determine the length of micro-strip transmission lines required in the design. However, the lateral MOSFET MRF826060HSR3 transistor require no matching process, as the input and output impedances are internally matched in the device. The following RT 5880 substrate specifications have been applied to achieve 21mm length of micro-strip line: $H =$

0.508mm, $\epsilon_r = 2.2$, $T = 3\mu\text{m}$, $\text{TanD} = 0.017$ and $z_0 = 50 \Omega$ [4].

B. Final Stage Power Amplifier Design

The design of power amplifier involves quite a few steps of design in order to ensure effective performance on the final device. It is however, important to note that optimization is applied in all stages of the design. In the bias circuit design a DC-feed (inductors) is provided in the drain and gate of the bias circuit to bias the transistor. This allows the DC current to pass through to the transistor, while the RF signal was blocked from passing to the DC bias. A lumped element was configured in the input and output of the amplifier, which acted as a DC-blocking capacitor. These elements blocked the DC voltage from the DC source to the RF line [4, 6].

In this work, input and output matching network have not been considered. The lateral LDMOS transistor is configured with internal matching network. To attain dynamic load variation, a quarter wavelength transmission line with 50 Ω impedance inverter was provided and a final class-AB power amplifier was designed. A 3dB quadrature coupler and a combiner was used in connecting the two class-AB amplifiers to provide a balanced power amplifier.

A balanced power amplifier linear simulation was conducted using Agilent advanced design system simulator (ADS) and result was obtained from 2.620 to 2.690GHz frequency band. The results have shown a good flat gain (S2,1) and outstanding return loss (S1,1) and (S2,2).

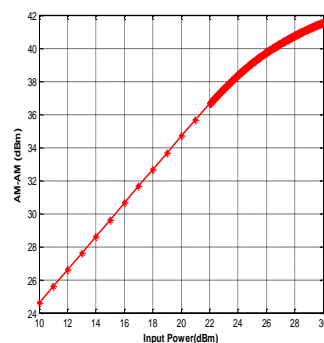


Fig. 3. AM-AM response.

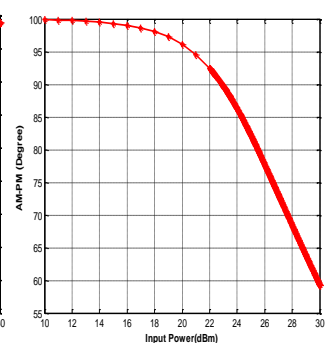


Fig. 4. AM-PM response.

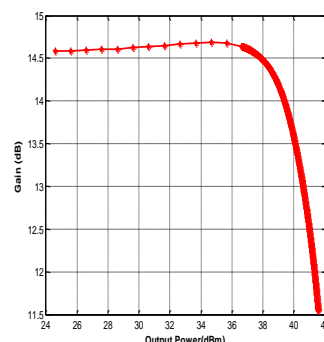


Fig. 5. Power gain.

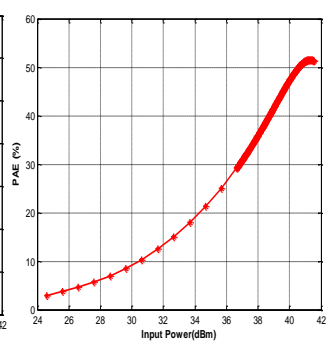


Fig. 6. Power added efficiency.

The balanced power amplifier nonlinear simulation was performed. The results were achieved based on single tone simulation and the following are the tests

performed, such as AM-AM, AM-PM, transducer power gain, output power and power added efficiency. Figure 3 and 4 represent amplitude and phase modulation responses [7, 8]. AM-AM characterization has demonstrated a variation of the input power versus the output power. The 40dBm output power is obtained at the safety region of 1dB compression point of the amplifier. While the AM-PM has shown the variation of phase from 100 degrees, decreasing at 1dB compression point. Figure 5 depicts a transducer power gain with a satisfactory gain of 14dB at 36dBm P_{out} . Figure 6 illustrates power added efficiency versus output power. The balanced power amplifier PAE goes up to 52% over the range of 41dBm P_{out} . The results demonstrated a significant upgrade by achieving such range of PAE in the design of the balanced power amplifiers [9, 10].

III. ADAPTING MODIFIED SALEH MODEL FOR ADAPTIVE DIGITAL PRE-DISTORTION IN MISO WLAN-OFDM TRANSCIVER

The balanced power amplifier designed for MISO WLAN-OFDM application using adaptive digital pre-distortion due to nonlinear distortions is presented. The amplitude and phase modulation distortions being the coefficients extracted from single tone simulations are characterize using MATLAB software platform. Curve fitting tool in MATLAB converts the amplitude and phase modulation coefficients to generate polynomials. The polynomials are used in developing the modified Saleh model algorithm for the adaptive digital pre-distortion system [8, 9].

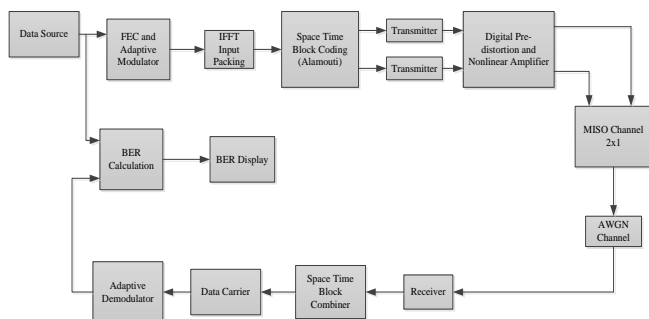


Fig. 7. MISO WLAN-OFDM Transceiver.

Figure 7 demonstrated the Simulink structure of wireless local area network IEEE 802.16 OFDM transceiver system configuration with coding support and BPSK, QPSK, 16-QAM or 64-QAM modulations. The transmitter is configured with space time block coding (STBC) for diversity. The STBC used Alamouti code at the downlink. However, this work focus on the digital pre-distortion and nonlinear amplifier block component of the transmitter [11]. The digital pre-distortion and nonlinear amplifier block consist of a circuit system. The subsystem model consists of several existing models such as Cubic Polynomial, Hyperbolic Tangent, Saleh Model, Ghorbani Model and Rapp Model [9, 12].

In Saleh model nonlinearity subsystem, a signal has been multiplied by a gain factor before splitting to magnitude and angle components. The magnitude

component is consist of the amplitude and phase respectively. AM-AM represents the amplitude, while AM-PM is the phase of the polynomials in Saleh model as shown in equation 1 and 2 [12].

$$AM - AM^u = \frac{\alpha u}{1 + \beta u^2} \quad (1)$$

$$AM - PM^u = \frac{\alpha u^2}{1 + \beta u^2} \quad (2)$$

To improve this model, a simple algorithm for linear equation was developed to characterize the AM-AM and AM-PM polynomials of the balanced power amplifier as shown is equation 3 and 4. It is applied in the adaptive digital pre-distortion to linearize the signal and compensate for the nonlinear distortion produced by the power amplifier [8].

$$x(t) = a_6 v^6 + a_5 v^5 + a_4 v^4 + a_3 v^3 + a_2 v^2 + av + a_0 \quad (3)$$

$$y(t) = b_6 u^6 + b_5 u^5 + b_4 u^4 + b_3 u^3 + b_2 u^2 + bu + b_0 \quad (4)$$

$$x(t) = am - am \quad (5)$$

$$y(t) = am - pm \quad (6)$$

To implement the transfer functions, the extracted data was measured in the environment of normalized input voltage against the output voltage of the balanced power amplifier. Figure 8 has shown the extracted data based on amplitude modulation, plotted with the following curve fittings: $a_6 = 33.066$, $a_5 = -85.52$, $a_4 = 82.06$, $a_3 = -34.052$, $a_2 = 2.85$, $a_1 = 3.21$ and $a_0 = -0.01$. The AM-AM characterization was effected by the device reaching a saturation point.

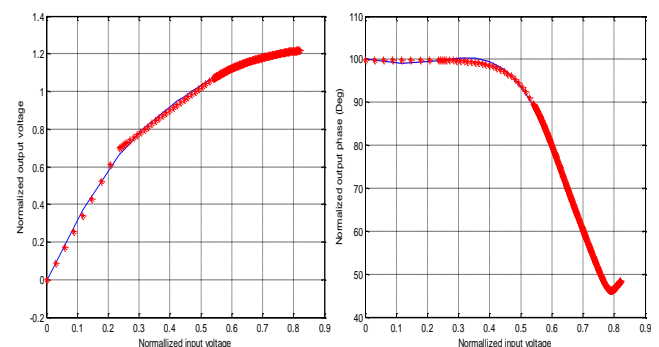


Fig. 8. Normalized amplitude. Fig. 9. Normalized phase.

The normalized input voltage versus output phase of the balanced amplifier was also considered in figure 9, plotted with the following curve fittings: $b_6 = 3.5485$, $b_5 = -5.7836$, $b_4 = 3.0384$, $b_3 = -0.8434$, $b_2 = 0.1826$, $b_1 = -0.0225$ and $b_0 = 0.1001$. The AM-PM characterization was effected by the device reaching a saturation point. Now, an accurate model by modified Saleh was developed to compensate for the nonlinear distortion and memory effect of the power amplifier. However, the adaptive digital pre-distortion algorithm was developed respectively. To evaluate the

performance of the pre-distorter, the balanced power amplifier was designed. The implemented balanced power amplifier in the context of amplitude and phase measured data was imported in a Simulink, developed based on IEEE 802.16 MISO WLAN-OFDM transceiver system.

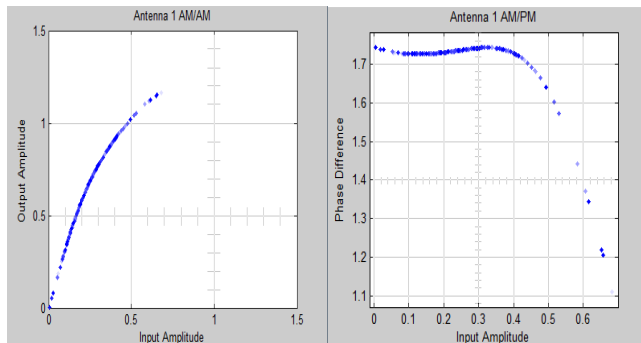


Fig. 10. AM-AM and AM-PM responses without linearization.

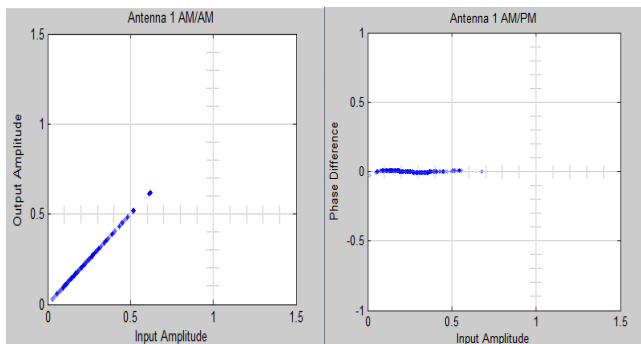


Fig. 11. AM-AM and AM-PM responses with linearization.

The memoryless nonlinearity performance of the modified Saleh model has been evaluated. Performance results of the transmitter is shown in figure 10 and 11. Figure 10 illustrates the amplitude and phase signals of the balanced power amplifier, reproduced by the transceiver system, without linearization. While figure 11 illustrates the amplitude and phase signals, linearized by the adaptive digital pre-distorter. Hence, the transceiver system was set to run on modified Saleh model with digital pre-distortion to compensate the nonlinearity of the balanced power amplifier.

Figure 12 illustrates the transceiver channel constellation for 16 and 64 QAM modulations. This is as a result bit error cancelation by the performance of the transceiver system. Gain vector of the MISO was increased, which triggers the adaptive rate control to set high the modulation from 16QAM to 64QAM. Signal to noise ratio was also increased from 21dB to 30dB to improve the constellation and remove the noise factor.

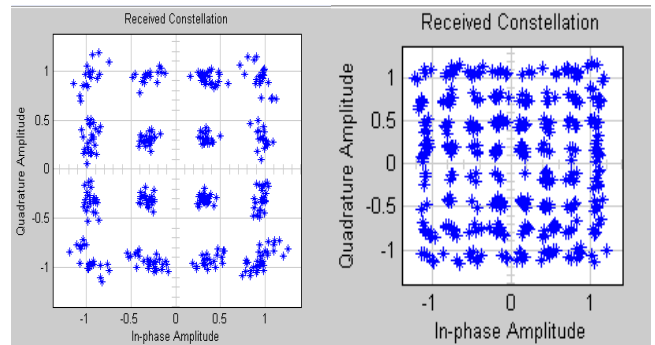


Fig. 12. 16QAM and 64QAM constellations.

IV. CONCLUSION

The balanced RF power amplifier was designed using Freescale N-Channel enhancement mode lateral MOSFET transistor. Linear and nonlinear simulation were performed with ADS simulator and performance result was obtained with acceptable power added efficiency of 52% for 41dBm output power at 1compression point. This paper conducts research on the effect of nonlinearity on Saleh model and the impact of digital pre-distortion. AM-AM and AM-PM characterizations were used on MATLAB to generate polynomials to model the balanced amplifier spectral re-growth using modified Saleh model. The memoryless nonlinearity has been compensated by the use of digital pre-distortion mechanism. This has proven that the simple linear by modified Saleh mode used in MATLAB Simulink, developed based on IEEE 802.16 MISO WLAN-OFDM transceiver system is capable of correcting nonlinear distortion and memory effects of the balanced power amplifier.

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