Journal of Multidisciplinary Engineering Science and Technology (JMEST)
ISSN: 2458-9403
Vol. 4 Issue 8, August - 2017

Digital Chronometer

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***Abstract*--During the developing period of technology, the accuracy of time is very impotant. That is haggling over every penny; therefore, the digital chronometer is very important for everyday life and industrial application. Example: Upon athletic field, it can measure the time of athletes. Upon industry, it can calculate the time needed among every productions and the crawling time for chemical pharmancy. Upon factory, it can measure the consume's time for every flow chart.**

This research paper can be divided into two parts. The first part is the counter of modulus 60 that is composed by decimal counter. When the frequency of digital impulse is adjusted to 1Hz, it becomes a second counter. The second part is the counter of modulus 60 too. When the sixtieth impulse of frontal second counter is coming, then the second part is going on, count from one, so that, it is a minute counter

Keywords—digital inpulse, frequency, modulus 60, second counter, minute counter

I. Introduction

The major objective of this research paper is to train the student about the flexible using of sequential logic by the least cost. The major structure of this research paper is decimal counter especially. We use the logic IC74LS90 under the flexible change to produce some features that we need.

II. Literature review

We can take some examples about counters in previous years. Zhuang Shengyan postgraduate study the ductility and reliability of counters in the literature [1] of his thesis of master degree. Yang Jingqi postgraduate study the automatic sensing of counters used for racing skating in the literature [2] of his thesis of master degree. He combine the automatic sensings and counters. Liu Liangyong postgraduate study electronic universal counters in the literature [3] of his thesis of master degree. He combine the counter by analog of electronic components.

III. Principle explanation

(1)We use the electronic components in this research paper have ①logic IC74LS90*4, 74LS47*4, 74LS08*2, 74LS32*2 ② electronic resistance 200Ω(1/4 W)*32 ③ common anode seven-segment LED monitor (small type)*4 ④ 3-point 2-segment sliding switch*1 ⑤ LED light*1 ⑥ circuit board *1 (numbering:EIC-1106) ⑦single core wire*1 (bundle)

(2)The total wiring diagram of this research paper is shown as figure(1).

(3)The SW(switch) is used as returning to zero of the counter in this research paper. When we set up SW=/ (5V), then, the chronometer is zero minutes and seconds. It's logic circuit is shown as figure(2). At the same time, CK4~CK1 have no effect at all (don't care), because this four IC7490s are washed away. The seven-segment LED displayer is denoted as 00:00

(4)The SW is set up to ϕ(0V) (grounded). The logic situation after the ninth trigger of CK4 is shown as figure(3). At that time $A_3A_2A_1A_0$ =/ϕϕ/$_{(2)}$=9$_{(10)}$, that is nine seconds and CK3=/(high potential). The seven-segment LED displayer is denoted as 00:09

(5)The SW is set up to ϕ(0V) (grounded). Under the temporality of the tenth trigger at CK4, IC7490(d) be reset again. By the way, because A_3:/→ϕ; therefore CK3 is resulting to negative-triggered. $A_7A_6A_5A_4$ =ϕϕϕ/$_{(2)}$=/$_{(10)}$. The seven segment LED displayer is denoted as 00:10. The logic situation is shown as Figure(4).

(6)The SW is set up to ϕ(0V) (grounded). The situation before the 60th trigger at CK4 is shown as figure(5). The seven segment LED displayer is denoted as 00:59. At the same time, CK3 is / (high potential)

(7)The SW is set up to ϕ(0V) (grounded). The first temporality after the 60th trigger at CK4 is shown as figure(6). IC7490(d) is reset again. It makes A_3:/→ϕ and A_0:/→ϕ; therefore, CK3:/→ϕ (negative triggered)

(8)The SW is set up to ϕ(0V) (grounded). The second temporality after the 60th trigger at CK4 is shown as figure(7). Because CK3:/→ϕ(negative triggered); therefore, A5:ϕ→/ and A4:/→ϕ

(9)The SW is set up to ϕ(0V) (grounded). The third temporality after the 60th trigger is shown as figure(8). Because the output of AND2 gate is transfered to /(high potential); therefore, the output of OR2 gate is transfered to /(high potential), IC7490(c) is cleaned and CK2 is transfered to /(high potential)

(10)The SW is set up to ϕ(0V) (grounded). The fourth temporality after the 60th trigger is shown as figure(9). Because A_5 is transfered to ϕ(grounded); therefore, the output of AND2 gate and OR2 gate are transfered to ϕ(grounded) simultaneously. Therefore, CK2: /→ϕ (negative triggered)

(11)Because the clock2(CK2) is negative-triggered in figure(9); therefore, A_8 is transfered to /(high potential) shown as figure(10). The seven segment LED displyer is denoted as 01:00

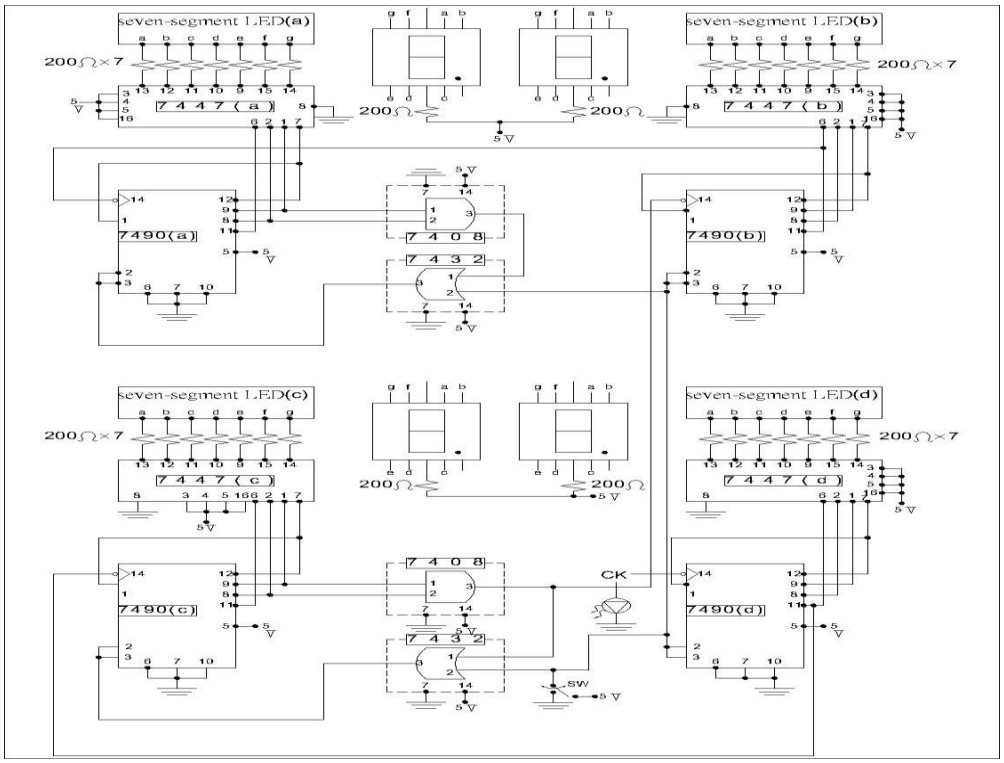

Fig.(1)the global diagram of the circuit

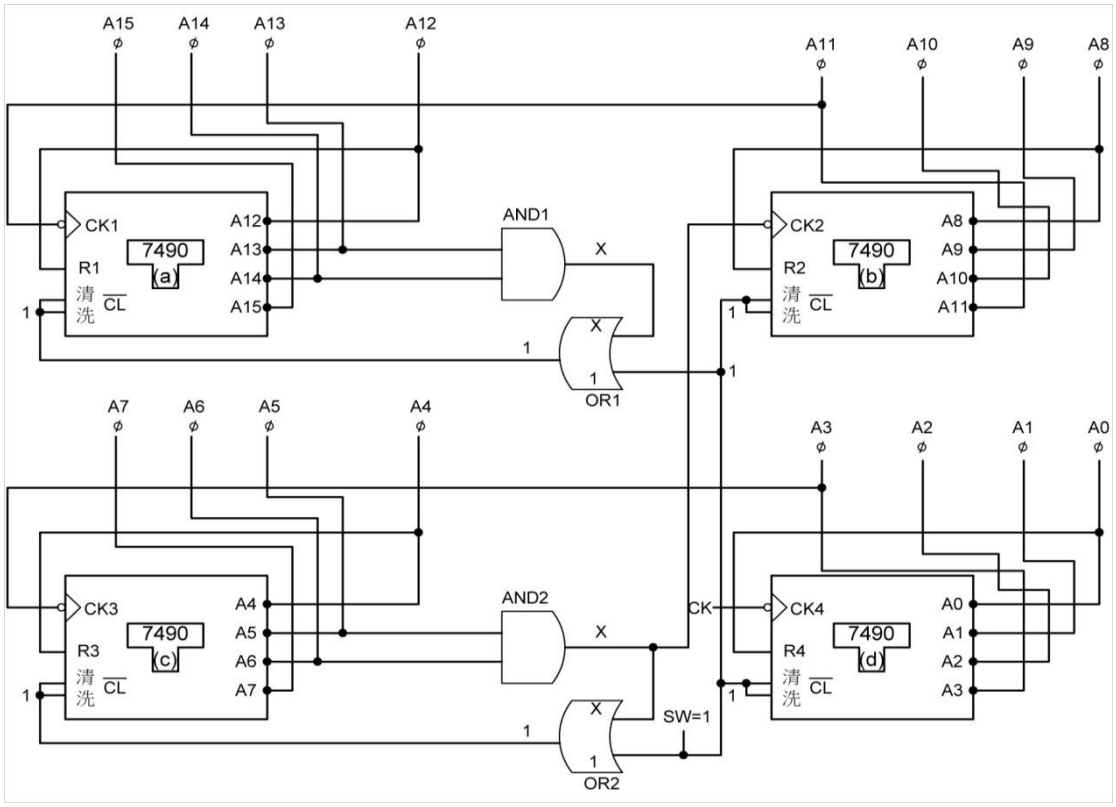

Fig.(2)the logic diagram in case of SW=/ (clearing)

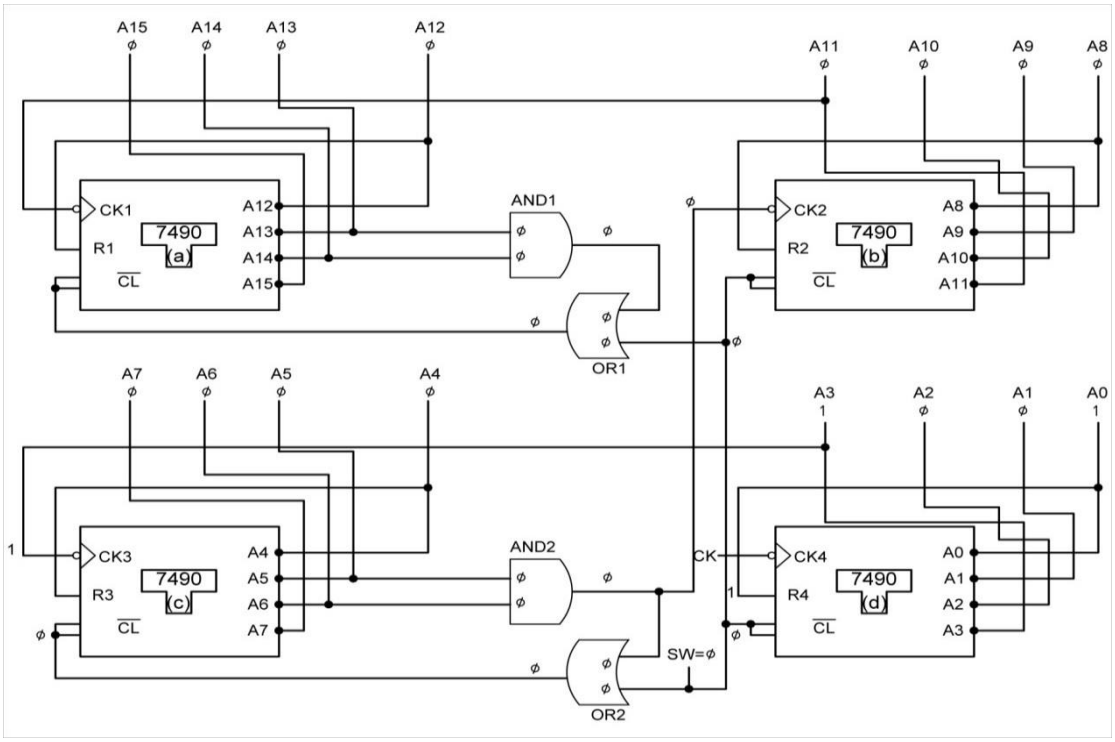

Fig.(3) the logic diagram after the ninth negative trigger at CK4

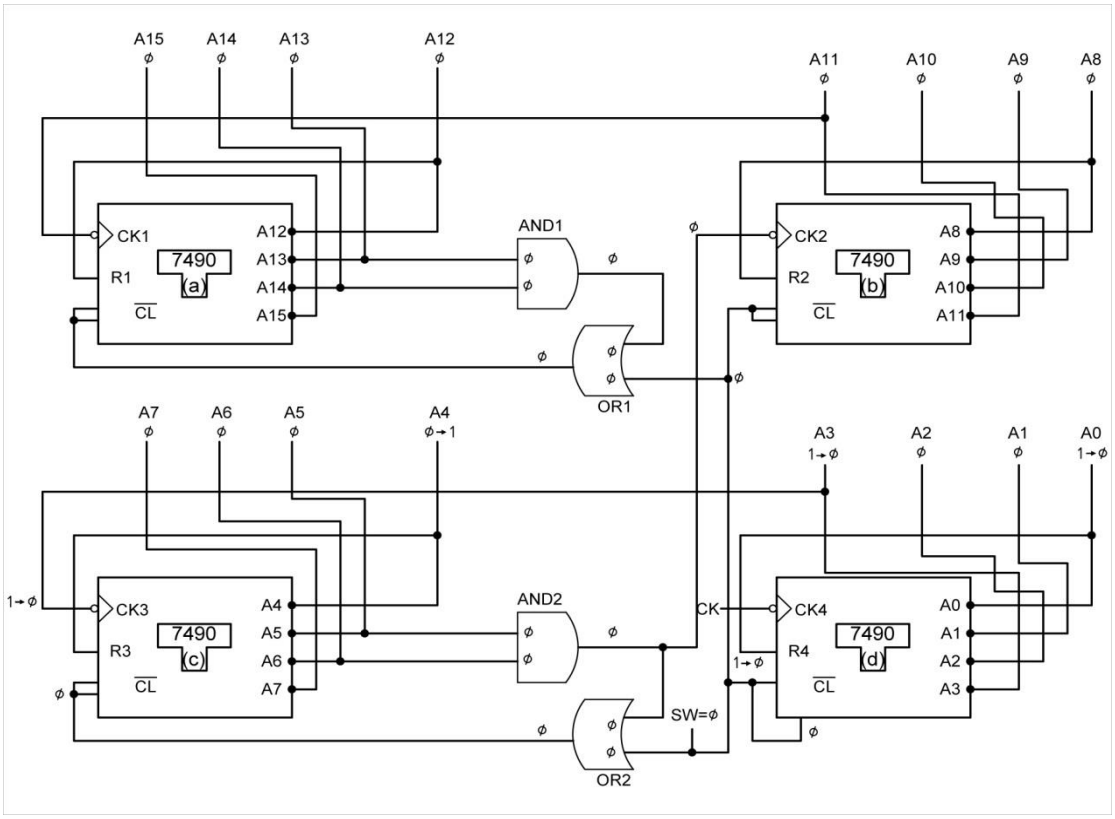

Fig.(4) the logic diagram after the tenth negative trigger at CK4

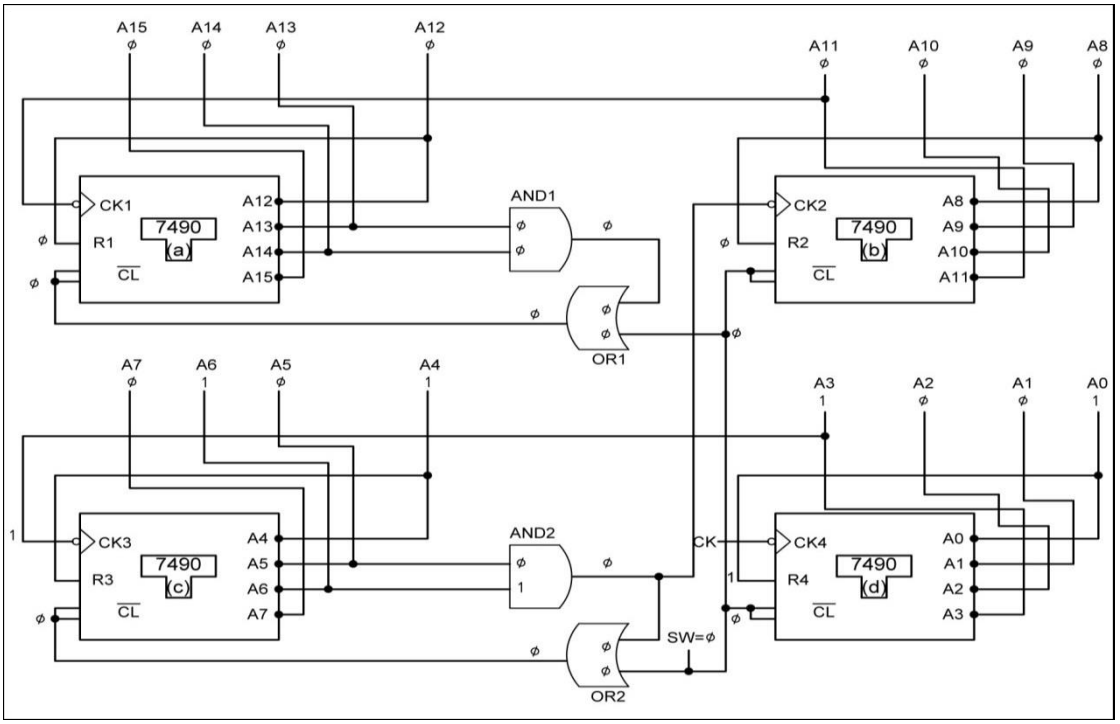

Fig.(5) the logic diagram before the sixtieth negative trigger at CK4

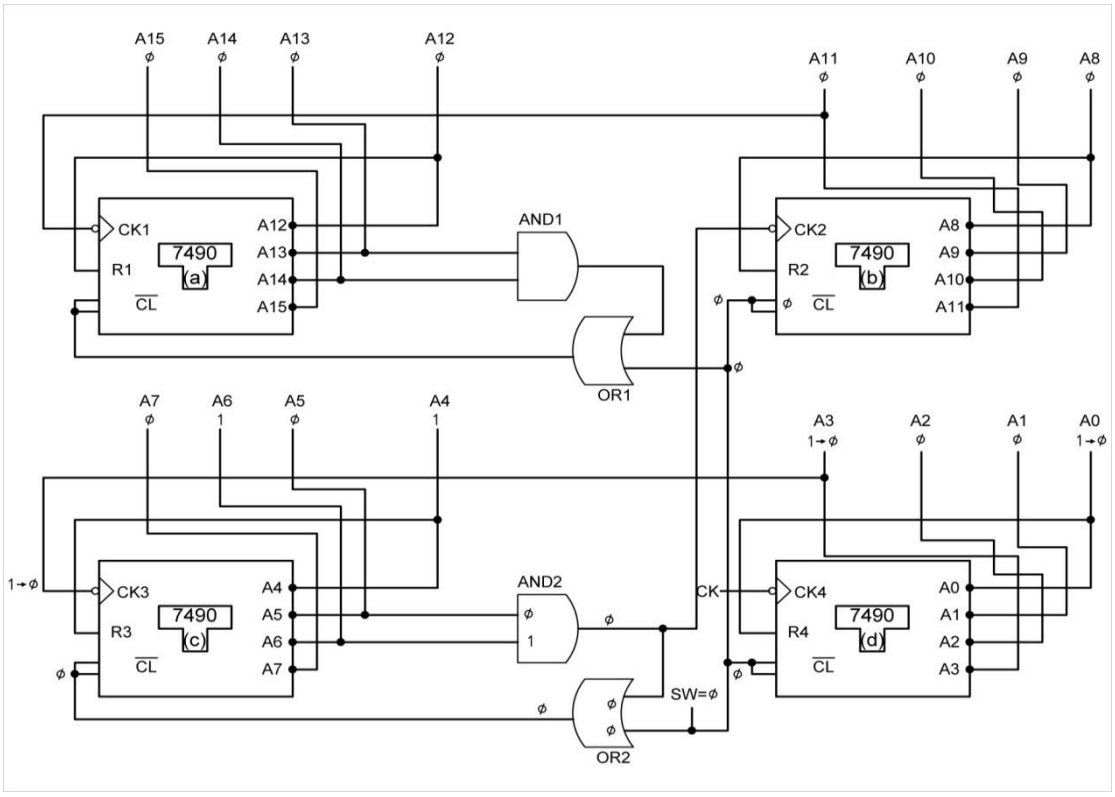

Fig.(6) the logic diagram of the first temporality after the sixtieth negative trigger at CK4

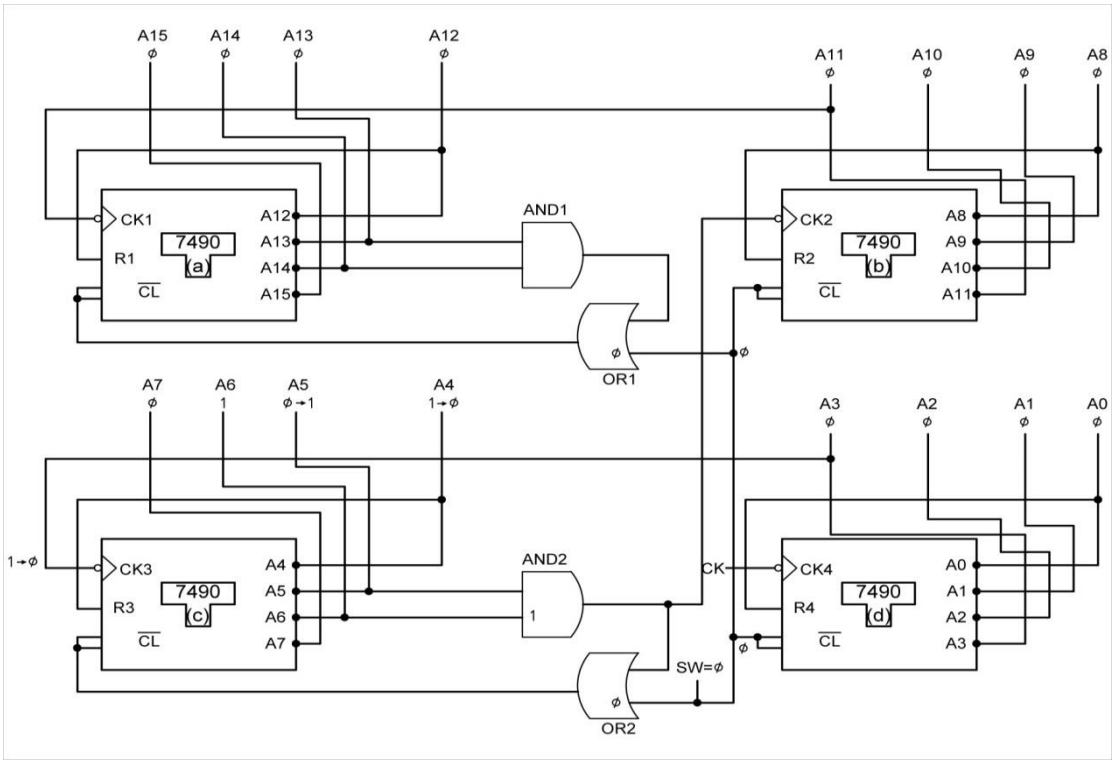

Fig.(7) the logic diagram of the second temporality after the sixtieth negative trigger at CK4

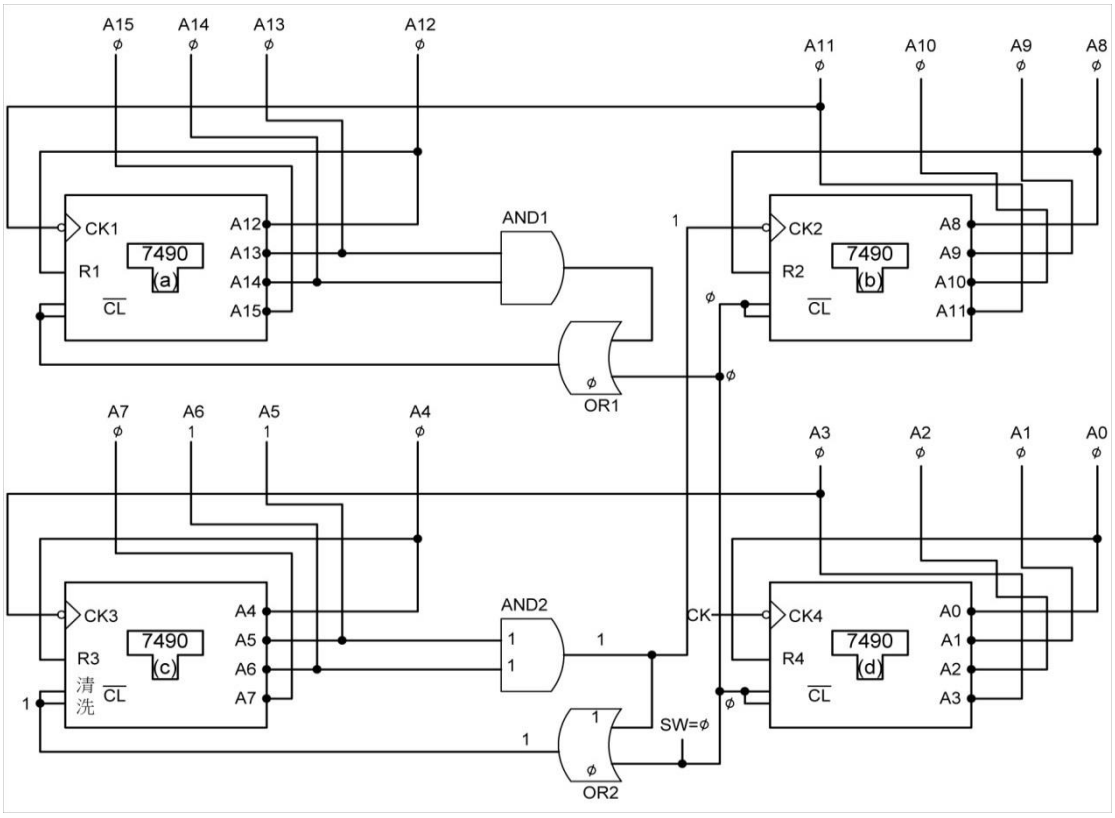

Fig.(8) the logic diagram of the third temporality after the sixtieth negative trigger at CK4

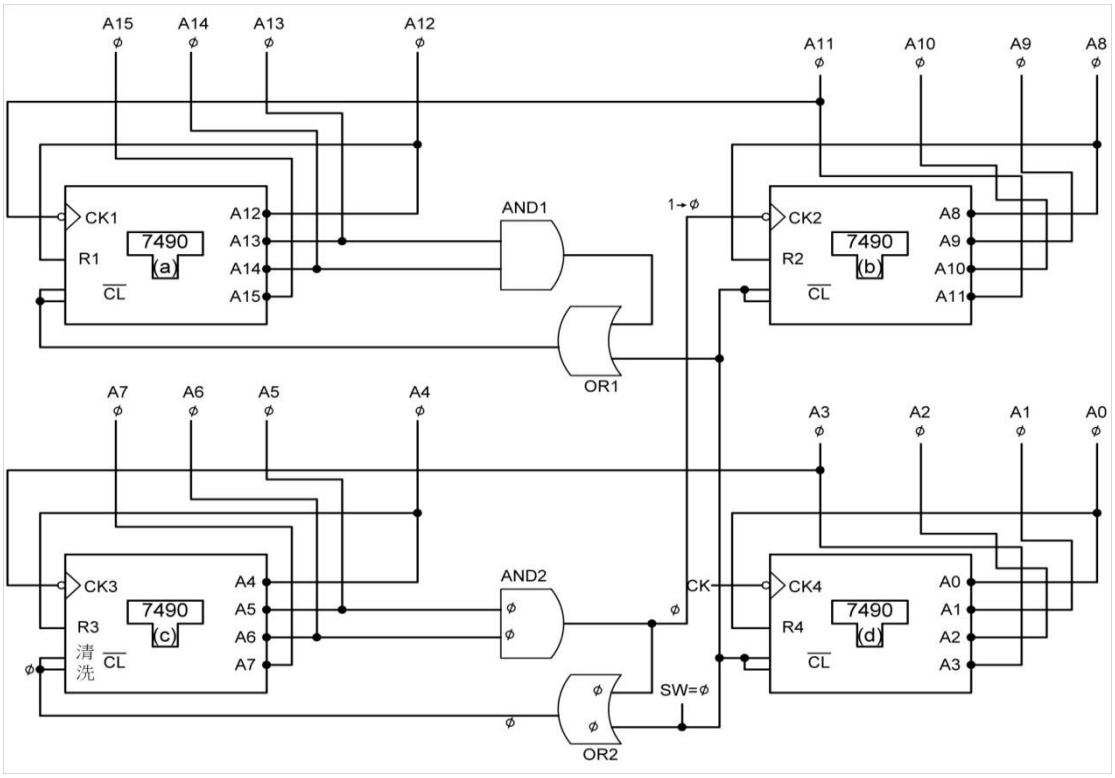

Fig.(9) the logic diagram of the fourth temporality after the sixtieth negative trigger at CK4

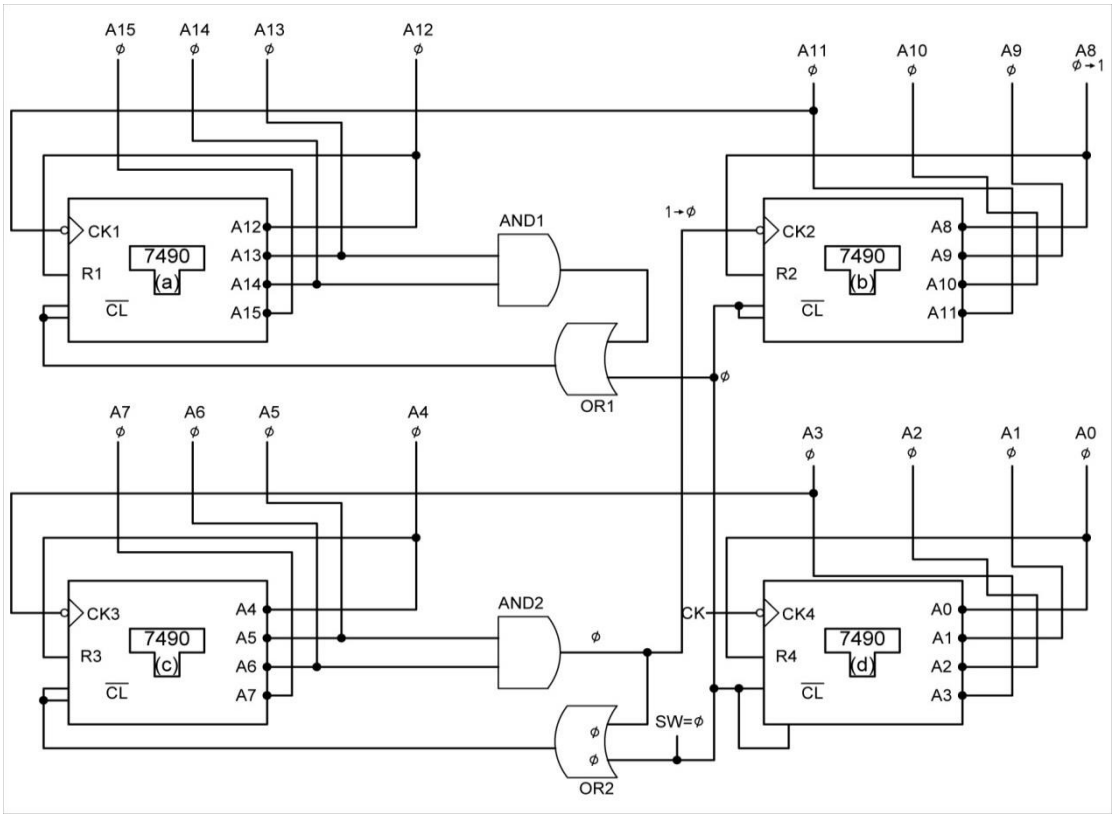

Fig.(10)the final diagram of logic after the sixtieth negative trigger at CK4

IV. Experimental result (truth table)

CK4	SW	minutes									seconds								
		A15	A14	A13	A12	A11	A10	A9	A8	顯示	A7	A6	A5	A4	A3	A2	A1	A0	顯示
×	1	×	×	×	×	×	×	×	×	00	×	×	×	×	×	×	×	×	00
1	0	ø	ø	ø	ø	ø	ø	ø	ø	00	ø	ø	ø	ø	ø	ø	ø	1	01
2	0	ø	ø	ø	ø	ø	ø	ø	ø	00	ø	ø	ø	ø	ø	ø	1	ø	02
3	0	ø	ø	ø	ø	ø	ø	ø	ø	00	ø	ø	ø	ø	ø	ø	1	1	03
⋮	0	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
10	0	ø	ø	ø	ø	ø	ø	ø	ø	00	ø	ø	ø	1	ø	ø	ø	ø	10
⋮	0	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
59	0	ø	ø	ø	ø	ø	ø	ø	ø	00	ø	1	ø	1	1	ø	ø	1	59
60	0	ø	ø	ø	ø	ø	ø	ø	1	01	ø	ø	ø	ø	ø	ø	ø	ø	00
⋮	0	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
522	0	ø	ø	ø	ø	1	ø	ø	ø	08	ø	1	ø	ø	ø	ø	1	ø	42
⋮	0	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
657	0	ø	ø	ø	1	ø	ø	ø	ø	10	ø	1	ø	1	ø	1	1	1	57
⋮	0	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1367	0	ø	ø	1	ø	ø	ø	1	ø	22	ø	1	ø	ø	ø	1	1	1	47
⋮	0	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
3117	0	ø	1	ø	1	ø	ø	ø	1	51	ø	1	ø	1	ø	1	1	1	57
⋮	0	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
3599	0	ø	1	ø	1	1	ø	ø	1	59	ø	1	ø	1	1	ø	ø	1	59
3600	0	ø	ø	ø	ø	ø	ø	ø	ø	00	ø	ø	ø	ø	ø	ø	ø	ø	00

Fig.(11) the truth table (symbol “X” denote don’t care)

V. conclusion

(1) Through the production of this paper, we can prove the wiring diagram of the logic circuit in figure (1) is correctly. Through the counting performance of BCD code in logic IC7490, we can get the cunting of 0~9.

(2) The performance of logic IC7408

(AND gate) is to carry out the action of modulus 60 in this paper. When the second number is achieveing 60; then, the chorometer can carry out 1 minute. When the minute number is achieveing 60; then, minute and second numbers are returned to zero simultaneous.

(3) The performance of logic IC7432 (OR gate) is to carry out the action of clearing in this paper. When the output of IC7432 is /(high potential); then, minute and second timers will be cleared.

(4) Because there are four IC7490s simultaneously in this paper; therefore, we mark with (a)(b)(c)(d) to avoid mistakes. These mistakes may guide to burn down the IC or short circuit.

VI. Reference

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