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Low Power Fully Differential Folded Cascode OTA with CMFB Circuit

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***Abstract*—This paper presents the designing of a fully differential folded cascode operational transconductance amplifier (OTA) with common mode feedback circuit (CMFB). The designed OTA is operated in sub-threshold region to reduce the power consumption. The simulation is carried out in CADENCE environment using 150nm CMOS. The simulation result shows the DC gain of 82 dB with UGBW of 768 KHz, CMRR of 128 dB and phase margin of 84 degrees. The power consumption of the OTA is 834.2nW. (*Abstract*)**

Keywords—operational transconductanc amplifier; Folded cascode; common mode feedback; sub-threshold; power consumption (key words)

I. INTRODUCTION (*Heading 1*)

Low power analog integrated circuits are playing an important role in portable and battery powered devices especially in biomedical equipment's and electronic gadgets [1]. Thus operating transistors in sub-threshold region is a good choice for IC designers [2]. OTA is one of the key building block which is extensively used in analog and mixed signal circuits [3]-[4]. It provides better linearity, low power consumption, better frequency response and less complexity of circuit [5].

There are many OTA structures discussed in literature [6]-[8] but single stage folded cascode OTA is one of the most common OTA topology that has high open loop gain and good frequency response [3]. Therefore, in this paper, a fully differential OTA is designed because fully differential structures suppress even harmonics which helps in producing reasonable THD but fully differential OTA structure requires a common mode feedback circuit to stabilize the common mode output because it is quite sensitive to the device properties and mismatches. Folded cascode operational transconductance amplifier with common mode feedback circuit is simulated in CADENCE environment. The DC gain, UGBW, phase margin, CMRR and power consumption is simulated as 82 dB, 768 KHz, 84 degrees, 128 dB and 834.2nW. The simulated input referred noise is 428.2uVrms The power consumption of the circuit shows the suitability of the circuit for low power applications.

Section I, is the introduction. Section II is divided into two parts, first part describes the OTA structure and the second part describes the common mode feedback circuit required for fully differential OTA. Section III shows the simulated result of different OTA parameters. Section IV concludes the paper.

II. OTA STRUCTURE

A. Folded Cascode OTA Design

The structure of folded cascode OTA is shown in Fig. 1. Majority of the noise contributors are basically the input devices. Therefore, PMOS is used as input differential pair because of its low flicker noise capability.

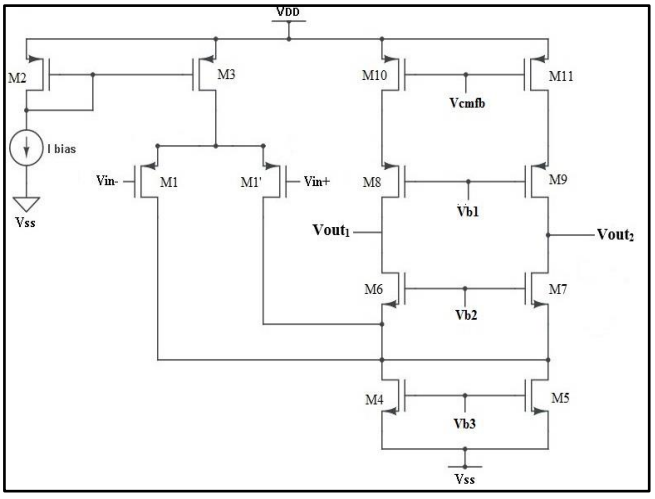

Fig. 1. Fully Differential Folded Cascode OTA structure

A fully differential architecture of folded cascode OTA is selected as it suppresses the even harmonics which are dominant in single ended OTA structure and also because of its higher common mode rejection ratio (CMRR) ad improved dynamic range [9]-[11]. The transistors are operated in sub-threshold region to reduce the power and make it suitable for low power applications. The biasing currents used are 100nA with a supply voltage of +/- 1V.

B. Common Mode Feedback Circuit (CMFB)

Fig. 2. shows the block diagram of the common mode feedback circuit (CMFB) required for the fully differential OTA structure. CMFB circuit performs three operations: it senses the common mode outputs of the fully differential OTA then compares the result with a reference voltage, normally the reference voltage (Vref) is equal to half of the supply voltage, for +/- supply voltage the reference voltage should be zero; and then returns the error to the amplifiers bias network (VCMC) using negative feedback to set the common mode (CM) output value [12]. The schematic of CMFB is shown in Fig. 3.

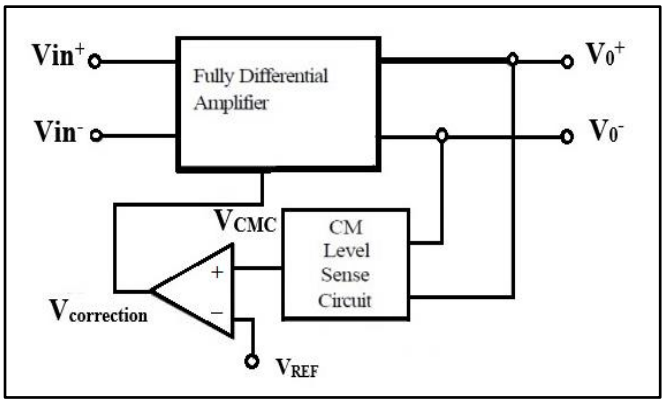

Fig. 2. Block diagram of Common mode feedback circuit

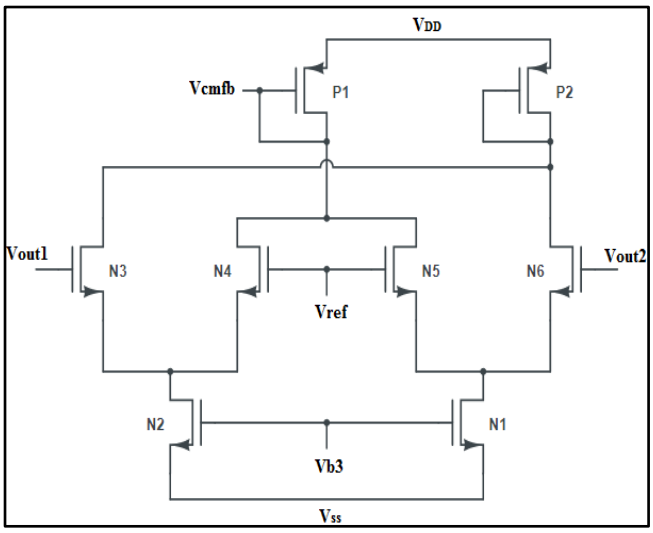

Fig. 3. Common mode feedback circuit

III. SIMULATION RESULTS

The simulations for the folded cascode OTA structure is carried out in CADENCE environment using 150nm CMOS technology. Fig.4. shows the simulated results for the gain, phase and unity gain bandwidth (UGBW). Fig. 5. shows CMRR graph and input referred noise plot is shown in Fig. 6.

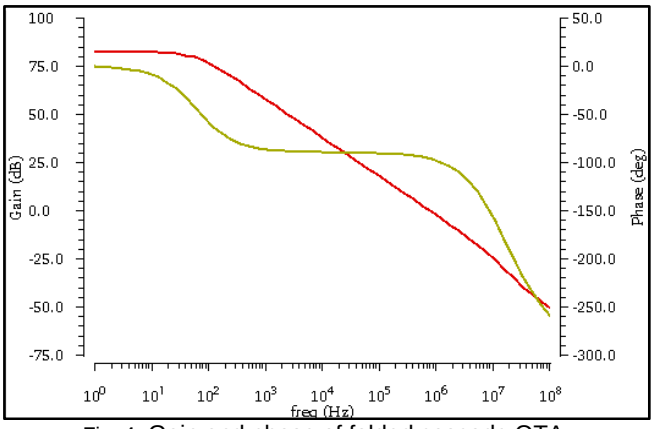

Fig. 4. Gain and phase of folded cascode OTA

The DC gain is 82 dB with phase margin of 84 degrees and UGBW of 768 KHz. The power dissipation of the circuit is 834.2nW which is suitable for low power applications. The OTA parameters and the aspect ratios of the transistors are tabulated in Table I and Table II respectively.

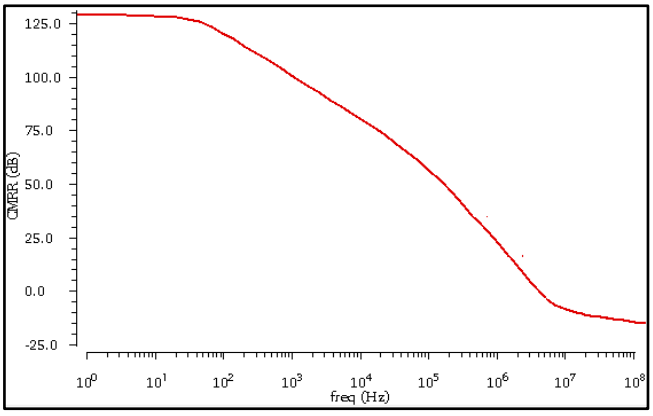

Fig. 5. CMRR of folded cascode OTA

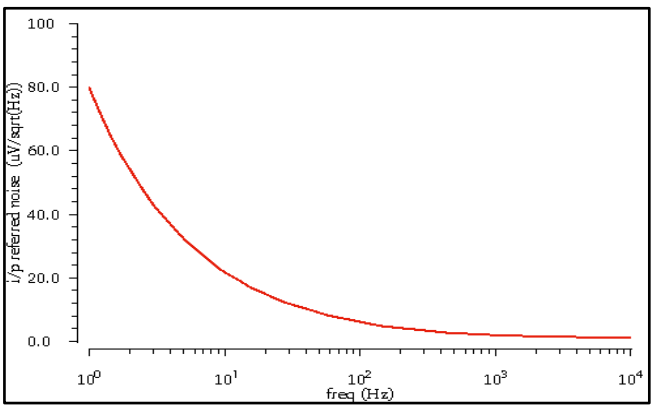

Fig. 6. Input referred noise plot in uV/sqrt(Hz)

TABLE I. DIFFERENT OTA PARAMETERS

Parameters	Values
Technology	150nm
Supply Voltage	+/- 1V
Gain	82 dB
Phase Margin	84^0
UGBW	768 KHz
CMRR	128 dB
Input ref. Noise	428.2uVrms
Power dissipation	834.2nW

TABLE II. ASPECT RATIOS FOR OTA TRANSISTOS

Transistors	W/L ratios
M1, M1'	10u/500n
M2,M3	4u/500n
M4,M5	8u/500n
M6,M7	4u/500n
M8,M9,M10,M11	4u/500n

IV. CONCLUSION

This paper describes the fully differential folded cascode OTA structures with common mode feedback circuit. This OTA is operated in sub-threshold region to reduce the power consumption. The input differential pair utilizes PMOS transistors to reduce the flicker noise which is less in PMOS compare to NMOS. The fully differential OTA structure requires a common mode feedback circuit to stabilize the common mode output because it is quite sensitive to the device properties and mismatches [13]. Different parameters of the OTA are simulated using 150nm CMOS technology in CADENCE environment. The power consumption of the circuit is in nano watt which is quite low and is suitable for low power applications.

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