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FPGA Based Waveform Generator and BIST unit for Binary Phase Coded Pulse Compression Radar

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***Abstract*—This work represents the design and implementation of a waveform generator and BIST (Built In Self-Test) unit for pulse compression radar using FPGA (Field Programmable Gate Array). The unit is capable of generating any binary phase coded waveform and testing a radar receiver by generating an echo like signal with predefined amplitude, range and Doppler shift.**

Keywords—FPGA; DDS; Barker Code

I. INTRODUCTION

A pulse compression radar transmits a special waveform and processes the received echo to provide high resolution in range and increased transmit power. Choosing the radar waveform is a crucial element for deciding the processing capabilities of the radar station. Waveform design is covered in detailed in [5] and is not the subject of this paper.

The transmitted waveforms used to be realized in old radar generations using analog devices [1], therefore it was very difficult and nearly impossible to generate highly complex radar waveforms such as nested Barker-169, also the matched filtering and pulse compression was carried out using analog tapped delay lines. In modern radar systems radar signal processing is undertaken digitally which provided more simple implementation of radar signal processing algorithms and allowed for more complex processing techniques to be realized in hardware.

In this paper we present a Field Programmable Gate Array Implementation (FPGA) of digital waveform and BIST (built in self-test) unit, the waveform generator is used for generating generic binary phase coded waveform with an IF frequency range up to 50 MHZ. the proposed BIST unit is capable of generating a fixed or moving echo's at different range cells to test the operation of the Radar DSP processor

II. DESIGN METHODOLOY

The digital circuit proposed consists of a waveform generator for the generation of the Binary Phase coded waveform using a Direct Digital synthesizer (DDS) IP core, multiplexers and comparators, this wave generator is also responsible for generating the sync pulse for the Radar.

The constant parameters for the waveform generator which is responsible for generating the pulse width, pulse repetition frequency and phase code are loaded to the circuit using universal asynchronous receiver/transmitter (UART). The design is optimized in hardware in order to be implemented in a single FPGA chip with the radar IF receiver and signal processor.

III. WAVEFORM GENERATOR

The waveform generator block design is shown in figure 1, the circuit consists of 2 parts, the PRI generator and the pulse generator.

A. PRI generator

The PRI generator consists of a counter comparator and a 2×1 multiplexer, the multiplexer inputs are the modulated pulse from the pulse generator and ground. The counter is basically a time counter that counts repeatedly from 0 to n_{PRI} where

$$n_{PRI} = \frac{PRT}{t_s}$$

The comparator compares the value of the counter with constant n_δ which represents the pulse width, if the counter value is greater than the pulse width, the comparator output is equal to one selecting the second output of the multiplexer.

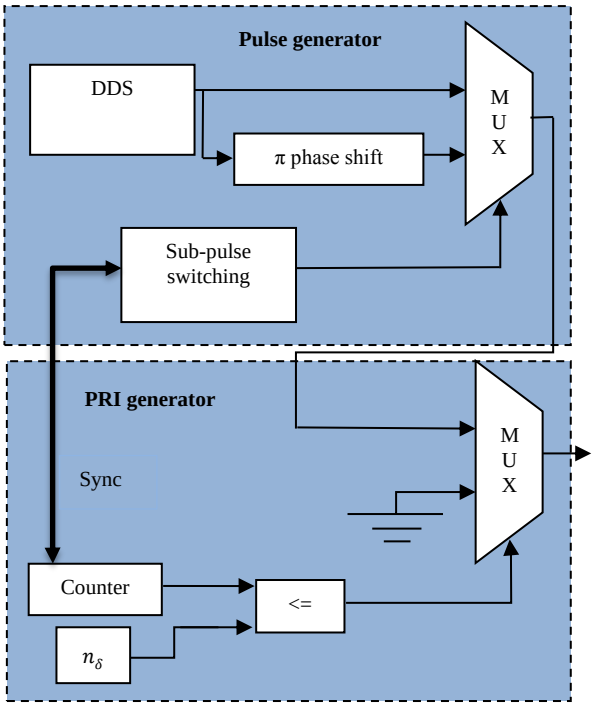


Fig. 1. *Waveform generator*

Therefore the multiplexer output is equal to the output of the pulse generator when the counter is less than or equal the pulse width, otherwise it is equal to zero.

B. Pulse generator

The pulse generator consists of DDS IP core, 180^0 phase shifting circuit, sub-pulse switching circuit, and multiplexer.

1) DDS:

The DDS IP core generates continues digital sine wave and cosine wave with the required frequency. The output frequency of the DDS is a function of the system clock, the phase width that is the number of bits $B(\theta(n))$ and the phase increment value $\Delta\theta$, the output frequency in Hertz is defined by:

$$f_{out} = \frac{f_{clk}\Delta\Theta}{B_{\Theta(n)}}$$

2) Phase shifting circuit:

In order to use the DDS to generate binary coded waveform, we need a sine wave and its negative for building the positive and negative sub pulses, since the DDS generates only sine wave and cosine wave, the output port is applied to a negating circuit to produce a 180° out of phase sine wave. The negating circuit or 180° phase shifting circuit consists of an inverter and constant 1 adding circuit, this circuit converts the digital word to its Two's complement value and therefore it phase shifts the complete waveform by 180°.

By applying both +Sine and –Sine as an input to a 2×1 multiplexer, different Barker code combinations can be generated. For example to generate a Barker 13 pulse waveform the selection of the multiplexer should be

0 0 0 0 0 1 1 0 0 1 0 1 0

Where each selection period is equal to the sub-pulse width. This multiplexer selection pattern is done by the sub-pulse switching circuit

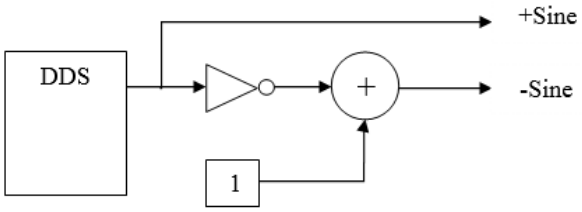
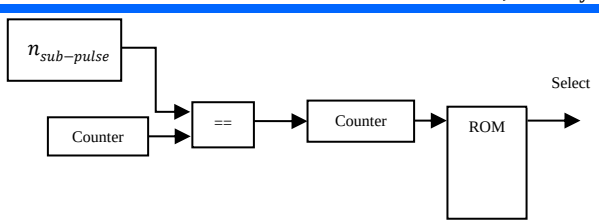


Fig. 2. π *phase shifting circuit*



3) Sub-pulse switching circuit:

The sub-pulse switching circuit is shown in figure 3, it consists of 2 counters comparator and a ROM, a constant $n_{sub-pulse}$ represents the number of samples in a single sub-pulse, when the first counter value is equal to $n_{sub-pulse}$ it resets to zero and enable a second counter to increment by 1. The second counter represents the address of the ROM storing the binary phase code in the form of binary 1 and binary 0.

IV. BUILT IN SELF-TEST UNIT

The BIST is designed to generate fixed echoes and moving echoes to test the Radar Moving target indicator (MTI) and detection capability, the range cell of the testing signal is changed by changing the sync pulse position. The DDS used in the waveform generation is used also for providing the reference sine and cosine signals for the coherent demodulator in the radar receiver therefore for generating a moving echo, a change in the phase between the testing echo signal and the reference signal must be done.

the sampling frequency is adjusted to $\frac{1}{8}$ of the IF frequency, i.e. for an IF frequency of 30 MHZ, a sampling frequency of 240 MHZ is used, therefore the single period is represented by 8 samples and 8 different phase shifts can be generated by adding a delay line consisting of 8 registers in front of the waveform generator.

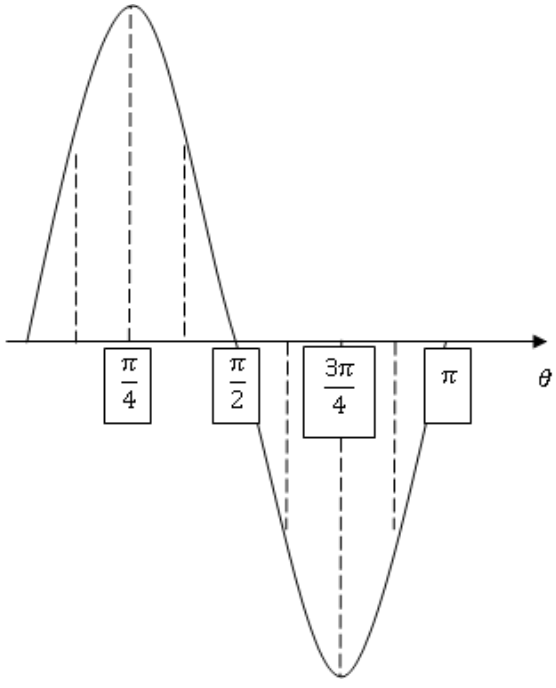


Fig. 3. *Discrete values constituting a single period*

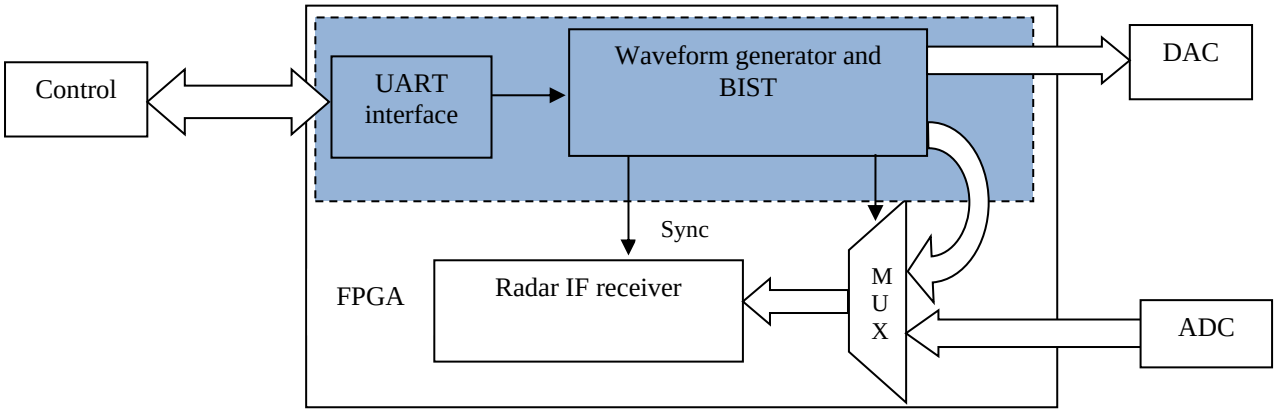


Fig. 4. *System level Block Diagram of the design*

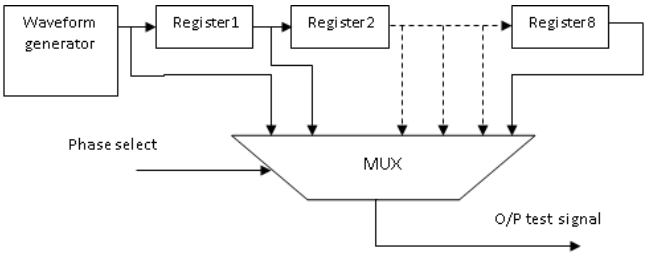


Fig. 5. *Moving echo generator*

The output of register 1 will be phase shifted by π/8, and the output of the second register in the delay line will be shifted by π/4, and the output of the third register will be delayed by 3π/8 and so on, as a result 8 different Doppler phase shifts can be obtained. The choice of the required phase shift is done using switches which represents the Phase select.

V. FPGA IMPLEMENTATION RESULTS

The paper emphasizes the implementation of the design using Field Programmable Gate Arrays (FPGA). The whole design explained above has been designed and optimized to fit in a single FPGA with the design of the Radar receiver.

Our design implementation uses VHDL coding and Xilinx IP cores and the software verification for the design has been carried out using a test bench written in VHDL to verify the operation using Modelsim software simulator. The next step was to implement the design on FPGA to be tested in real hardware, the Xilinx ML605 FPGA board was used as the target device for the hardware verification. The ML605 contains Vertix6 XC6VLX240T FPGA and it's suitable for signal processing applications. The system has been designed to consume a small amount of the chip resources to allow the implementation of radar signal processor in the same chip with the waveform generator.

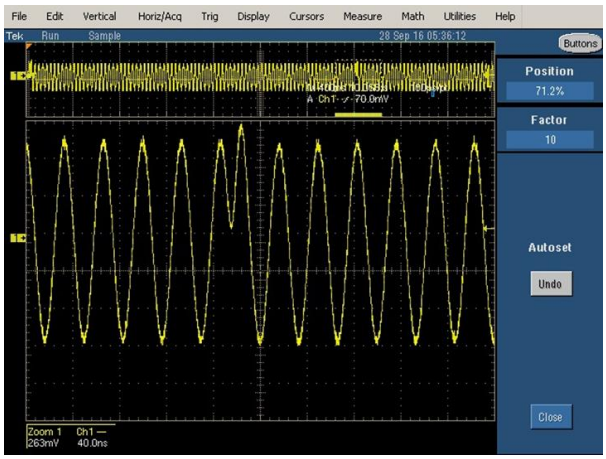


Fig. 6. *Binary phase coded waveform generated by FPGA*

The proposed design consumes less than 1% from the total resources of the chosen target device with an operating frequency up to 260 MHZ.

The 16 bit output of the waveform generator is connected to the DAC3283 dual channel 16-bit 800Msps DAC available in the DSP150 data acquisition card, Fig 7 shows the results on oscilloscope for Nested Barker 169 waveform with a sub-pulse width of 0.6 μs and a total pulse-width of 104 μs, the figure shows the complete pulse on the upper axis and the phase difference between sub pulses on the lower axis.

TABLE I. DESIGN SUMMARY

Logic Utilization	Device utilization summary		
	used	***available***	***utilization***
Slice Registers	68	301440	0%
Slice LUTs	163	150720	0%
RAMB361	2	416	1%

CONCLUSION

The paper explains in details the hardware implementation of a digital waveform generator for binary phase coded pulse compression radar. The method used in the design facilitates the generation of complex phase coded pulse waveforms such as the Nested Barker 169. The constant values representing the IF frequency, pulse width, pulse repetition interval and Barker code are loaded to the circuit using UART interface giving a simple method to modify the Radar waveform parameters and can be controlled automatically from PC for anti-jamming purpose.

The utilization of the customized cores in the design models delivers high level of performance and area efficiency. Thus it resulted in an efficient implementation of the hardware using less percentage of FPGA resources. In addition, digital implementation is advantageous because the system becomes highly flexible, simple and reliable.

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