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The Concept Of Memory Device Diagnosis Algorithm Design

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Abstract **- The high-performance memory device fault-detection automated test design techniques and measures are suggested. For designing the algorithms and testing programs the object's and testing device's simulation models allowing to save project operations labor are designed.**

Keywords—automated designing; memory; operational processors; tests

I. INTRODUCTION

Better performance of distributed system requires more complicated structure and architecture of modern semiconductor memory chips. DDR and QDR memory chips imply writing and reading data burst having length up to 8 words. To the execution of high-performance memory device diagnostics during the stage of designing multiprocessor structure, containing several groups of address code formers, testing tools are effectually.

The significant contribute to setting the theoretic and practical bases of semiconductor memory device diagnostics was made by Ivanyuk A.A., Hahanov V.I., Yarmolik V.I., Suk D.S., Reddy S.M., Yan de Goor A.J., Zorian Y.Y. et al [1, 2]. Nevertheless in most sources of literature descriptions of algorithms and tests' behavior are presented, but the principles of test design and description of used tools are not presented fully. High-performance memory device diagnostic testing program design requires high labor coefficient and consumes much time and material resources thus designing of new testing time reducing techniques and tools is required.

II. OBJECT

Of the article is designing of techniques and tools of high-performance memory device automated diagnostic test.

Operator format of algorithms is used to display memory device diagnostic operations [3-5]. Writing zero to (a) address storage register operation displays V(a) operator, writing one does W(a) and reading data - R(a). Filling all storage registers with one on increasing address code can be introduced as a sequence of operators $\mathop{\mathbf{P}}_{a=0}^{n-1} W(a)$ with P determining sequence of executed operations, the lower index is for initial value of storage register address and the upper one is for final address of storage registers. Sequence of writing zero to all storage registers operations on decreasing address code can be introduced as a sequence of operators $\mathop{\mathbf{P}}_{a=n-1}^{0} V(a)$. Data reading operations can be formulated as $\mathop{\mathbf{P}}_{a=0}^{n-1} R(a)$ in case of increasing address code and $\mathop{\mathbf{P}}_{a=n-1}^{0} R(a)$ otherwise.

The algorithm of March_LA test can be formulated as a sequence of operations:

$$\pi_{march\_LA} = \mathop{P}_{a=0}^{n-1} V(a) \mathop{P}_{a=0}^{n-1} (R(a)W(a)V(a)W(a)R(a)) \cdot \mathop{P}_{a=0}^{n-1} (R(a)V(a)W(a)V(a)R(a)) \mathop{P}_{a=n-1}^{0} (R(a)W(a)V(a)W(a)R(a)) \cdot \mathop{P}_{a=n-1}^{0} (R(a)V(a)W(a)V(a)R(a)) \mathop{P}_{a=n-1}^{0} R(a)$$

The task of designing of algorithm of the test can be split into separate sub-tasks and on completing them the fulfillment of further conditions is required:

a) $\forall\, a,\ a = \overline{0, n-1}$ Complete write zero operation V(a);

b) $\forall\, a, a = \overline{0, n-1}$ complete 5 memory operations to (R(a)W(a)V(a)W(a)R(a));

c) $\forall\, a,\ a = \overline{0, n-1}$ complete further operations (R(a)V(a)W(a)V(a)R(a));

d) $\forall\, a,\ a = \overline{n-1, 0}$ complete 5 memory operation to (R(a)W(a)V(a)W(a)Ra) on decreasing address code;

e) $\forall\, a,\ a = \overline{n-1, 0}$ complete sequence of further operations (R(a)V(a)W(a)V(a)R(a));

f) $\forall a, a = \overline{n-1, 0}$ Complete reading data R(a) and matching it with master value equal to zero.

The program model of the object and diagnostic tools designed according to the following rules helps to reduce algorithms and testing programs design labor coefficient.

Rule 1. A 16x16 matrix exploring by four operation processors is used as an object of diagnosis. The storage registers are enumerated from 0 to 255.

Rule 2. The limitation of operation processors scrolling are two matrix points with initial coordinates gx, gy and last coordinates nx,ny.

Rule 3. Micro operations $x_r := gx$, $y_r := gy$ are required for setting *r*-element of operation processors in position of exploring initial cell with coordinates *gx* and *gy*.

Rule 4. Micro operations $x_r := nx$, $y_r := ny$ are required for setting *r*-element of operation processors in position of exploring last cell with coordinates *nx* and *ny*.

Rule 5. With regard to the rules 3 and 4 the following operation processor position change set is used:

$$O_r^x = \{(x_r := x_r); (x_r := gx) : (x_r := nx); (x_r := x_r \pm 1); (x_r := x_r \pm 2); (x_r := x_r \pm 3);$$
$$(x_r := x_r \pm 4)\}; O_r^y = \{(y_r := y_r); (y_r := gy) : (y_r := ny); (y_r := y_r \pm 1); (y_r := y_r \pm 2);$$
$$(y_r := y_r \pm 3); (y_r := y_r \pm 4); (y_r := y_r \pm 1)^*\}$$

with symbol * standing for carried or borrowed bit from coordinate X.

Rule 6. Six conditional branch flags for each operation processors are used to programming control device state transition

$$F = \{(x_r \neq gx); (y_r \neq gy); (x_r \neq gx) \vee (y_r \neq gy);$$
$$(x_r \neq nx); (y_r \neq ny); (x_r \neq nx) \vee (y_r \neq ny)\}$$

Rule 7. With regard to the rule 6 the following control device change set is used:

$$Q = \{Q := Pon(x_r \neq gx); Q := Pon(y_r \neq gy); Q := Pon(x_r \neq gx) \vee (y_r \neq gy);$$
$$Q := Pon(x_r \neq nx); Q := Pon(y_r \neq ny); Q := Pon(x_r \neq nx) \vee (y_r \neq ny)\}$$

with P standing for branching address.

Rule 8. The setting error flag E micro operation is provided for matching exploring cell value and master value by the following condition:

$$\forall r, r = \overline{0.3}V = \begin{cases} if\ S_r \neq S_e\ then\ E := 1 \\ else\ E := 0 \\ endif \end{cases}$$

with S_r standing for exploring value and S_e for master value.

Rule 9. With regard for the rule 8 control device displays an error message on E=1.

The block schematic diagram of the model of the object and control device consists of the matrix of 256 cells, control device (CP) and four operation processors H0-H3 (Fig. 1).

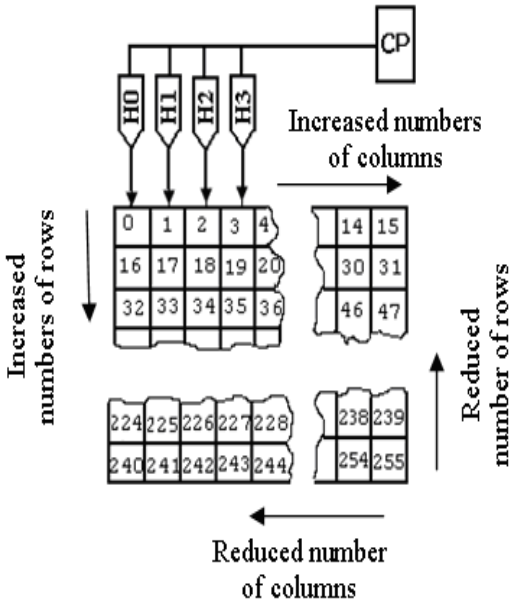

Fig 1. The block schematic diagram of the model of the object and diagnostics tool.

The suggested mathematical model is defined by five components:

$M = \langle Q, q_0, S, p_r, \delta \rangle$,

with Q is for control device set of states; q_0 for control device initial state; S for alphabetic character set; p_r for r-element of operation processors coordinates incremental value; δ for transition function showing subset of class $Q \times (S^r \times p^r)$.

Solution of the subtask (a) and (f) of the March_LA test doesn't present difficulties, but it's necessary to rearrange the algorithm for generation the number of cycle operations multiple to the number of the operation processors (four) and of fragment of the algorithm (five) for solution the subtask (b). The minimal number meeting the conditions is 20.

The sequence of operation of the subtask (b) after the rearrangement is presented in table 1.

Table 1. The sequence of operations of the subtask (b)

The number of OP	The value of OP	Cycle operations				
		1	2	3	4	5
0	0	R(0)	R(0)	W(1)	V(2)	W(3)
1	1	W(0)	R(1)	R(1)	W(2)	V(3)
2	0	V(0)	W(1)	R(2)	R(2)	W(3)
3	1	W(0)	V(1)	W(2)	R(3)	R(3)

On execution of the cycle operations micro operations should be formed in a manner as to the

operation processors take the needed positions and generate data to process by the algorithm. Data alteration micro operations of the subtask (b) are presented in table 2.

Table 2. Data alteration micro operations of the subtask (b)

The number of OP	The value of OP	Cycle operations				
		1	2	3	4	5
0	0	⌉		⌉	⌉	⌉
1	1	⌉	⌉		⌉	⌉
2	0	⌉	⌉	⌉		⌉
3	1	⌉	⌉	⌉	⌉	

In table 2 the symbol ⌉ corresponds to data inversion operation.

The cell address code change operation should be executed to solve the subtask (b). The micro operations are presented in table 3.

Table 3. The cell address code change operation

The number of OP	The value of OP	Cycle operations				
		1	2	3	4	5
0	0		+1	+1	+1	+1
1	0	+1		+1	+1	+1
2	0	+1	+1		+1	+1
3	0	+1	+1	+1		+1

In table 3 the symbol +1 corresponds to address code increment by one.

The operation processors should be configured in such a way as to start exploring from zero cell (fig 2) to scan the cells in address code ascending order on completing the subtasks (b) and (c) of March_LA test.

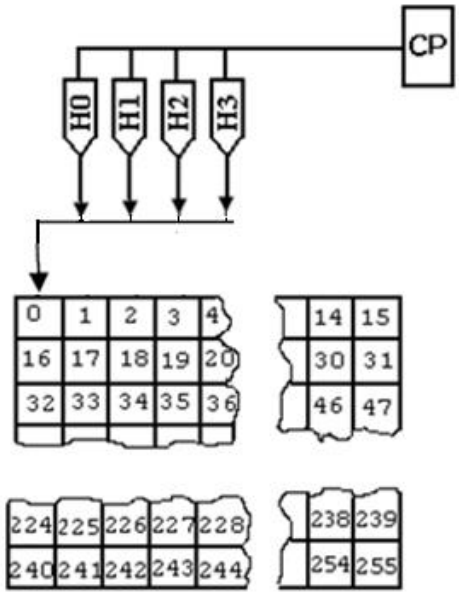

Fig 2. The initial configuration of operation processors on completing subtask (b) and (c).

The operation processors should be configured in such way as to start exploring from the last cell (fig. 3) to scan the cells in address code descending order on completing subtasks (d) and (e). The operations of subtasks (b) - (e) should be executed 64 times for 256 bit memory device testing.

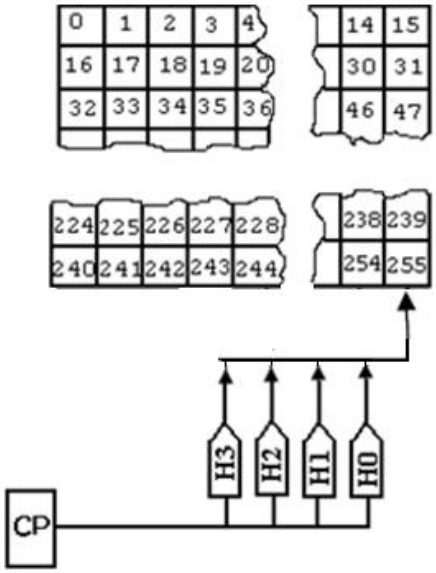

Fig 3. The initial configuration of operation processors on completing subtasks (d) and (e).

One should lay down logical-analytical conditions for algorithm and testing programs providing memory device access without throttling. That allows increasing fault detecting chance. In case of the operation processors symbols in neighboring steps are not equal $S_r^i \neq S_r^{i+1}$ the data code inversion should be executed $t_r^i := \neg t_r^i$. If positions of operation processors are not the same in neighboring steps $p_r^i \neq p_r^{i+1}$ then the operation processors swap micro operations $a_r^i := a_r^i + (a_r^{i+1} - a_r^i)$ are required.

Solving of each subtask requires $m = Q * l$ number of operator with Q standing for number of operations in a subtask. Testing of *n* bit memory device requires executing of each subtask $j = \frac{n}{l}$ times.

If the designed algorithm meets the previously mentioned logical-analytical conditions then memory device access operations will be executed on operating frequency without throttling. Otherwise the test duration will increase with sacrifice in throttling increasing time of switching of address decoder. All these factors decrease test validity.

The algorithm design general methodology is confined in completing of the further tasks [6-8]:

a) Selection of pattern generation coefficient for defined memory device. Determination of number of operation processors;

b) Analyzing vector algorithm and defining of operations number order by number of operation processors;

c) Configuration the algorithm in the way that number of storage access operations in cycle is multiple to the number of operation processors;

d) Defining the number of repeating of separate pieces of the algorithm and selection of micro operations for each cycle;

e) Task decomposition: designing of algorithm and its optimization via Prover framework for 256 bit memory device;

f) Establishing program variables - memory size function;

g) Designing the algorithm via transformation of the functional depending variables for new type of memory device.

CONCLUSIONS

The designed memory device and diagnostic tools program model can be used in engineering and scientific-production associations and in universities for developing new diagnostic systems.

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