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Design and Implementation of High Performance, Low Dead Zone Phase Frequency Detector in CMOS PLL based Frequency Synthesizer for Wireless Applications

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***Abstract*— An area efficient, high performance, low dead zone phase frequency detector for high frequency phase-locked loop is presented in this paper. We have designed and developed the phase frequency detector circuit using 180nm process technology in CADENCE Virtuoso Analog Design Environment. The various performance parameters have been obtained through different types of simulation. While designing we have worked on mainly power supply, power dissipation, wide input frequency range, dead zone size and active layout area. The basic PFD consumes 33.5 µW at 500 MHz operating frequency whereas the proposed PFD with GDI cell consumes only 8 µW at 5GHz. The simulation results show that the circuit offered an alternative for any high speed and low power PLL applications.**

Keywords—CADENCE, CP, Dead zone, GDI, low power, PLL, PFD, VCO.

I. INTRODUCTION

Phase-locked loops (PLLs) are mostly used in radio frequency synthesis. The PLL based frequency synthesizer is one of the main building blocks of an RF front-end transceiver. The PLL frequency synthesizer system is mainly designed to ensure the accuracy of its output frequency under operating conditions. The goal to meet strict phase noise, spurious-level performance and fine frequency resolution with Low Power CMOS Phase-Locked Loop Synthesizers reasonable levels of power consumption remains a challenging task for the circuit designer [1].
Fig. 1 depicts a PLL-based integer-N frequency synthesizer. It consists of a phase-frequency detector, a charge-pump, a loop filter, a voltage-controlled oscillator, and a programmable frequency divider. For an integer-N frequency synthesizer, the output frequency is a multiple of the reference frequency:

$$f_{out} = N. \ f_{ref} \quad (1)$$

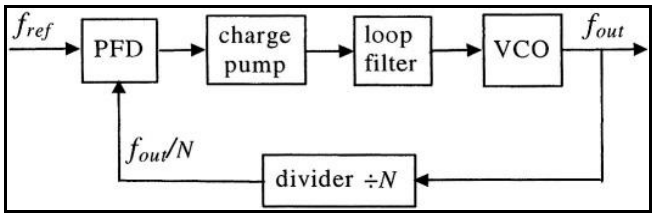

Fig 1: *Integer-N PLL-Frequency Synthesizer*

where N, is an integer, the loop frequency divide ratio. The frequency resolution of the integer-N frequency synthesizer is equal to the reference frequency. For narrow-band applications, the reference of the synthesizer is very small and the frequency divide ratio is very large because of the limitation of frequency resolution equal to the reference frequency. The first component of the PLL is the Phase Frequency Detector which has been designed to improve the speed by minimizing the dead zone.

This paper presents the design and implementation of high performance, low dead zone, phase frequency detector in CMOS PLL based frequency synthesizer for wireless applications. Section II presents the analysis and design of phase frequency detector. PFD with Gate Diffusion Input Cells is presented in Section III. Simulation Results are discussed in Section IV. Section V provides the circuit layout and the performance analysis of both PFD circuits. Finally, Section VI presents the discussion and conclusion of the proposed work.

II. PHASE FREQUENCY DETECTOR

A PLL is a feedback system that compares the output phase with the input phase. The comparison is performed by a phase comparator or a phase detector. A familiar example of phase detector (PD) is the exclusive OR (XOR) gate As the phase difference between the inputs varies, so does the width of the output pulses, thereby providing a dc level proportional to the phase difference (Δϕ). The XOR PD produces error pulses on both rising and falling edges. A simple D flip-flop (D-FF) could also be used as a phase detector. Here, the reference signal serves as a clock to sample the divided VCO signal. When reference leads the feedback divider signal, the output remains at logic '1' and if the reference lags the feedback divider signal, the output switches to logic '0'. Therefore, the D-FF based PD operation is highly nonlinear and leads to the stability issue and phase error. This PD also fails to detect any frequency difference.

A. Tri-State Phase Frequency Detector Analysis and Design

The XOR and DFF based PDs fail to detect the frequency difference and are not suitable for PLL applications where initial VCO oscillation frequencies are far away from reference. A tri-state PFD detects both phase and frequency difference. Fig. 2 [2] shows the state diagram and the implementation of the PFD.

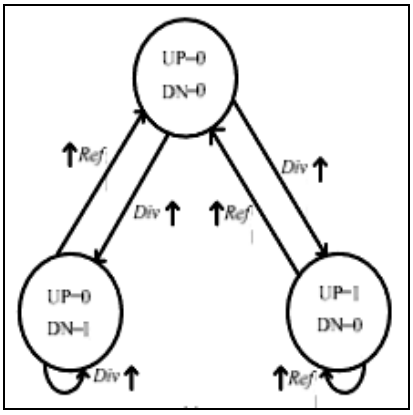

Fig.2: Tri-state PFD a) State diagram

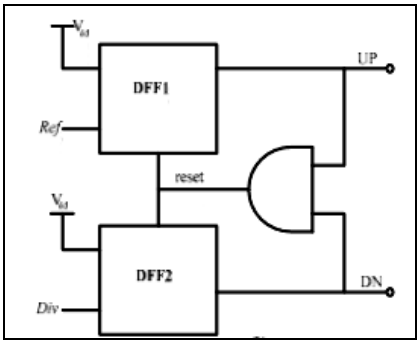

Fig.2: Tri-state PFD b) Implementation

Let Ref be the reference signal, and Div the divider output signal. If Ref leads Div, the rising edge of Ref triggers DFF1 and the UP signal is switched from 0 to 1 and DN signal remains at 0. The UP signal remains at 1 until the occurrence of rising edge of Div which triggers DFF1 and the UP signal is reset to 0 by the AND gate. A similar behaviour happens when Ref lags Div. The phase difference between Ref and Div is indicated by the difference between UP and DN signals. Fig. 3 shows the transfer characteristics of a tri-state PFD which is unsymmetrical over y-axis and the output has the same sign as that of the phase.

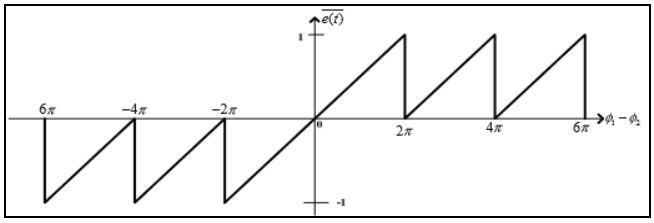

Fig.3. Transfer characteristics of a Tri-state PFD

difference. Therefore, the output would be in opposite polarities between positive and negative frequency difference. When Ref leads Div (Ref f > Div f), the resulting positive pulses appear at UP while DN stays at 0. When Ref lags Div (Ref f < Div f), the resulting positive pulses appear at DN while UP stays at 0. Thus, the average of UP-DN suggests the frequency difference [3].

B. Dead zone in tri-state PFD

Moreover, tri-state PFD suffers from the "dead zone" problem. Dead zone is defined as the maximum difference in phase between the two inputs that cannot be detected by a PFD. The transfer function curve under the dead zone is given in Fig.4. When the phase difference between Ref and Div is close to zero, the width of the UP and DN pulses would approach to a minimal, which is set by the delay of the AND gate in the feedback path. However, the charge pump may not be to detect such narrow pulses, resulting to no current injecting to the LPF, which is almost similar to the case of zero phase difference. As a result, the PFD gain is down to zero and the PLL loop would not function and there would be an unpredictable phase error between the two inputs so the jitter at output of the PLL accumulates. The dead zone in the PFD is avoided by introducing delay after the AND gate in the feedback path to increase the propagation delay as shown in Fig. 4.

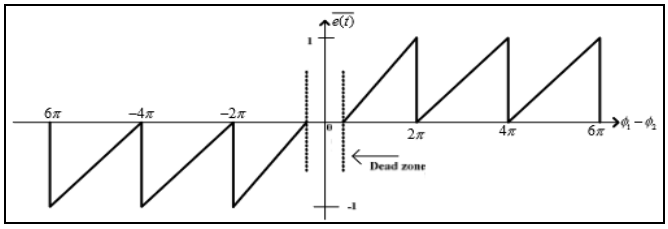

Fig.4: Dead zone in tri-state PFD

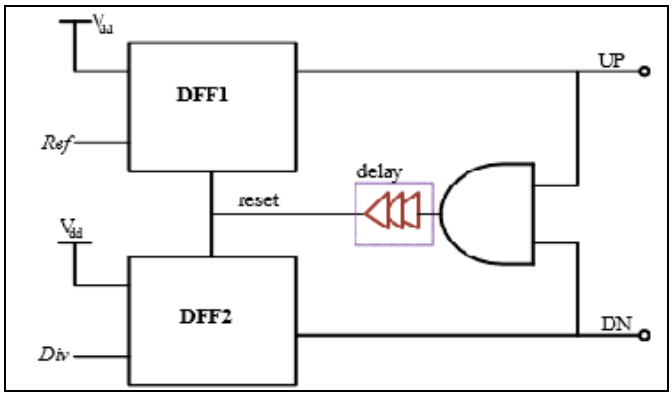

Fig.5: Dead zone free PFD

The Tri-state PFD is designed using two D Flip flops with reset. The D Flip flop is made by pass transistor logic and a buffer to make it faster and compact and it will work at 1 GHz as shown in Fig. 5. The PFD is designed and tested up to 1.2GHz frequency as the input signal. The tri-state PFD is used because it is simple, has linear phase-detecting range of +/-2π radians, is duty-cycle insensitive and can act both as a phase detector and as a frequency detector [3].

The design consists of two D flip-flops and a AND gate in the reset path to reset both the flip flop. The schematic of the D flip-flops and the PFD are shown in fig. 6 and fig. 7 respectively. The undetectable small phase range called as dead zone influences the effective sensitivity of a PFD. To minimize the power consumption of the PFD, it is must to reduce the reset path delay so that dead zone can be minimized [4, 5]. In order to avoid dead-zone a useful equation for the minimum reset delay of the PFD is given by following equation:

$$T_{reset} = T_{th} = (T_r + T_f)/2 \quad (2)$$

where T_{th} is the charge pump switching time and can be approximated by the average of the rise time T. The delay time of logic components and reset time of feedback path of flip-flop causes a PFD to detect phase and frequency with distortion [6].

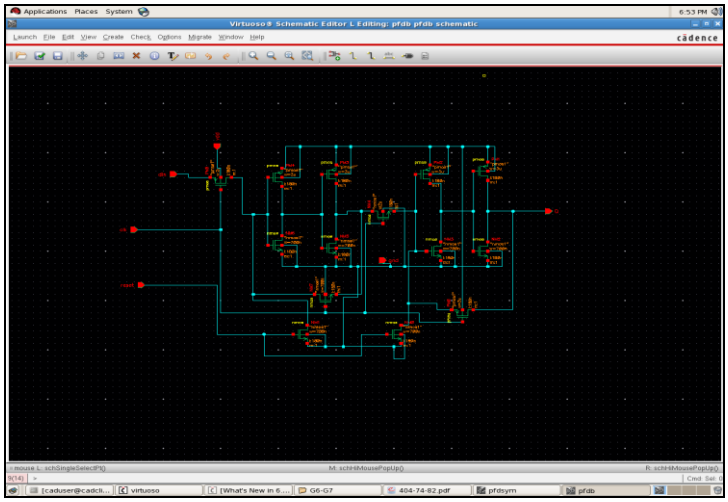

Fig.6: Schematic of D - flip flop

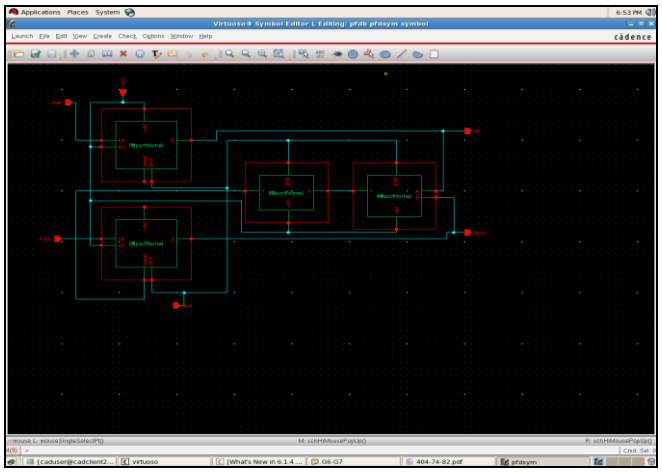

Fig 7: Schematic of PFD

III. PFD WITH GATE DIFFUSION INPUT CELLS

The circuit diagram of proposed Gate Diffusion Input Cells (GDI) is as shown in below fig. 8. It works similar to conventional PFDs but it has many advantages compared to conventional PFDs. This PFDs is basically constructed with two GDI cells. A basic GDI cell contains four terminals – G (common gate input of nMOS and pMOS transistors), P (the outer diffusion node of pMOS transistor), N (the outer diffusion node of nMOS transistor), and D (common diffusion node of both transistors) .This technique allows reducing power consumption, propagation delay and area of digital circuits. The GDI method is based on the simple cell shown in fig 9. Table1 shows how different logic functions can be implemented with GDI cell.

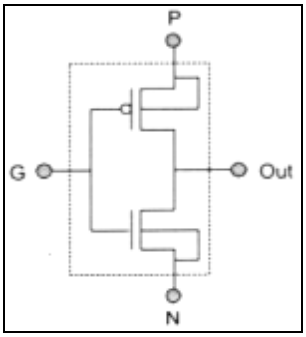

Fig.8: Basic GDI Cell

Table I: Logic Functions implemented with GDI cell

N	P	G	D	Function
„0“	B	A	A“B	F1
B	„1'	A	A“+B	F2
„1“	B	A	A+B	OR
B	„0“	A	AB	AND
C	B	A	A“B+ A C	MUX
„0“	„1“	A	A“	NOT

when Fclk is equal to Fvco both the outputs that is Up and Down are zero, if Fclk is high compared to Fvco then up signal is high else down signal is high indicating the phase error between Fclk and Fvco. The conditions of inputs and outputs are depicted in state machine diagram shown in fig. 9

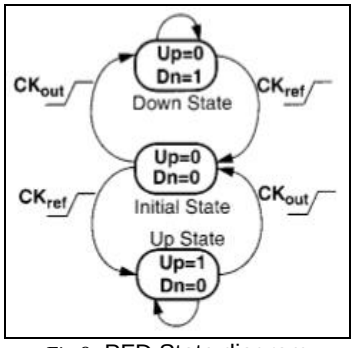

Fig.9: PFD State diagram

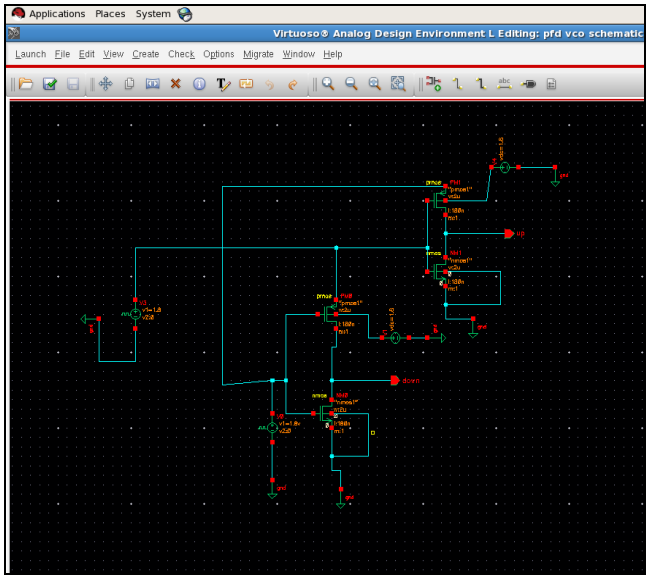

Fig.10: Schematic of PFD with GDI cells

The schematic of PFD with GDI cells is given in fig. 10. It can be observed from this schematic that the PFD design using GDI has less complex hardware it than the conventional PFD. Hence, it requires less on-chip area.

IV. Simulation Results

A. *Conventional PFD*

Transient analysis of PFD is carried out for three different conditions as shown fig 11. The waveforms obtained shows that the designed PFD fulfils required operation. The up and down pulses are obtained depending on inputs to it which can be applied to charge pump as input. All n-channel devices have a width of 700nm, and all p-channel devices have a width of 3µm. VDD is chosen to be 1.8 V for CMOS latch. All simulations are performed by using Cadence spectre simulator.

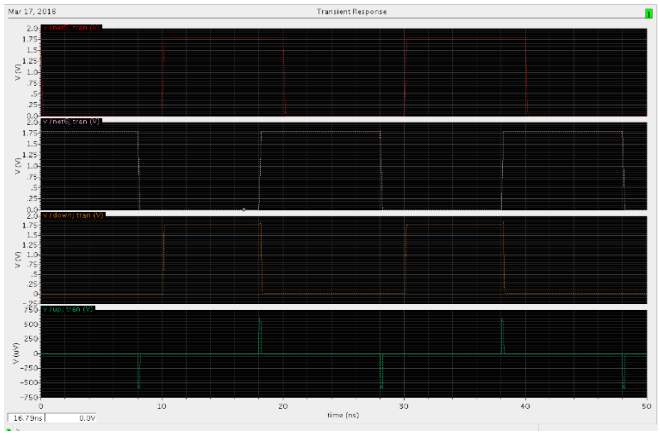

Fig. 11: a) Output of PFD when Feedback signal leading reference signal

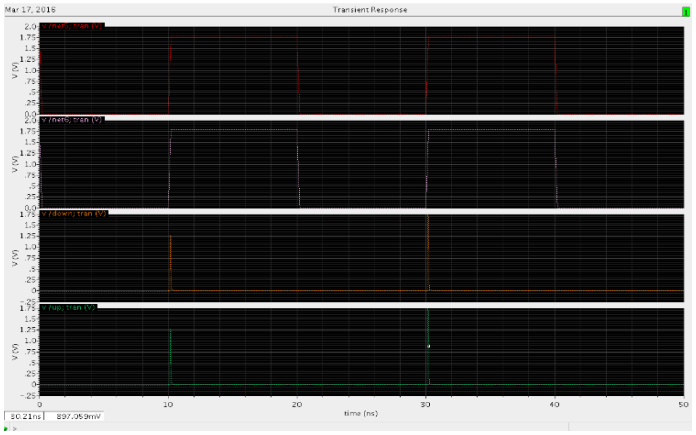

Fig.11: b) Output of PFD when Feedback signal in phase with reference signal

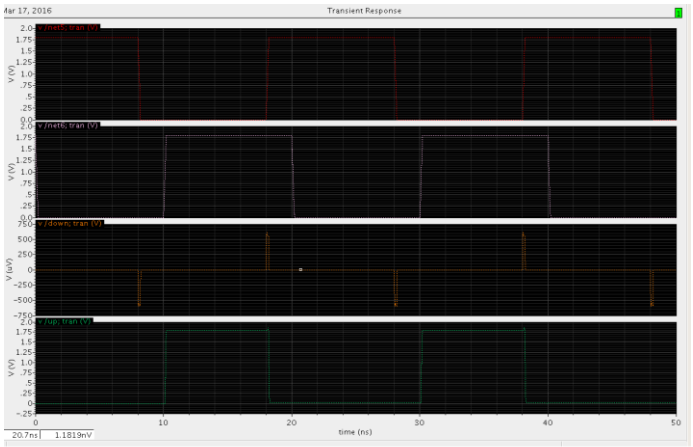

Fig.11 : c) Output of PFD when Feedback signal lagging reference signal

B. *PFD with GDI cells*

The phase frequency detector has been designed to implement the PLL at 5 GHz and simulated by Virtuoso Cadence Spectre for low dead zone, small area and low power consumption. The output of PFD with GDI cells is shown in fig 12. The pulse illustrating phase difference is shown with UP signal with green colour. This circuit can be used in the application on high frequency, low dead zone and low power phase locked loop.

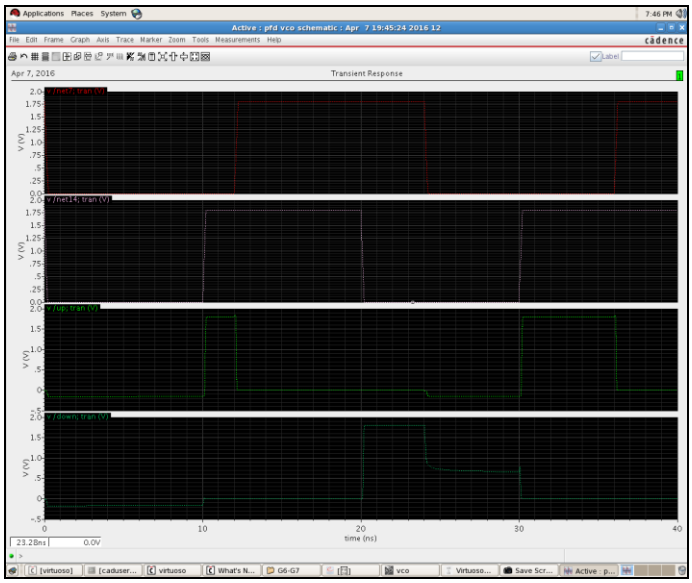

Fig.12: Output of PFD with GDI cells

Fig. 13 shows a longer simulation done on proposed PFD. The input CLK frequency is 500 MHz with Fclk leading Fvco by 20ps; this will result in having UP signal as we can see from the graph. This PFD were able to operate at much higher frequency 5GHZ is the highest frequency the PFD will operate at. Even at the phase difference of 20ps between Fclk and Fvco the proposed PFD is able to detect the difference which is depicted in fig. 13.

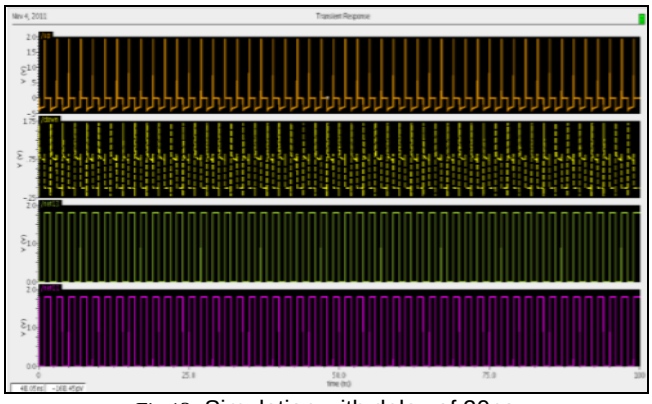

Fig.13: Simulation with delay of 20ps

V. CIRCUIT LAYOUT AND PERFORMANCE ANALYSIS

Virtuoso is the main layout editor of Cadence design tools. The phase frequency detector is implemented using Cadence Virtuoso 0.18µm technology. Fig. 14 illustrates the layout of the conventional tri-state PFD. Layout of phase frequency detector with GDI cells are depicted in fig. 15. As shown, this PFD requires less on-chip area as compared to the conventional tri-state PFD**.** The performance comparison between both PFD topologies is shown in table.2. Layout versus Schematic (LVS) comparison ensures that the layout actually implements the required functionality. If the extraction program allows to extract also parasitic from the layout view, a more accurate, Post-Layout Simulation, can be performed taking into account the geometry of the circuit. The created mask layout must conform to a complex set of design rules, in order to ensure a lower probability of fabrication defects. A tool built into the Layout Editor, called Design Rule Checker (DRC), is used to detect any design rule violations during and after the mask layout design. Proposed Design shown in fig. 14 and 15 has clear DRC.

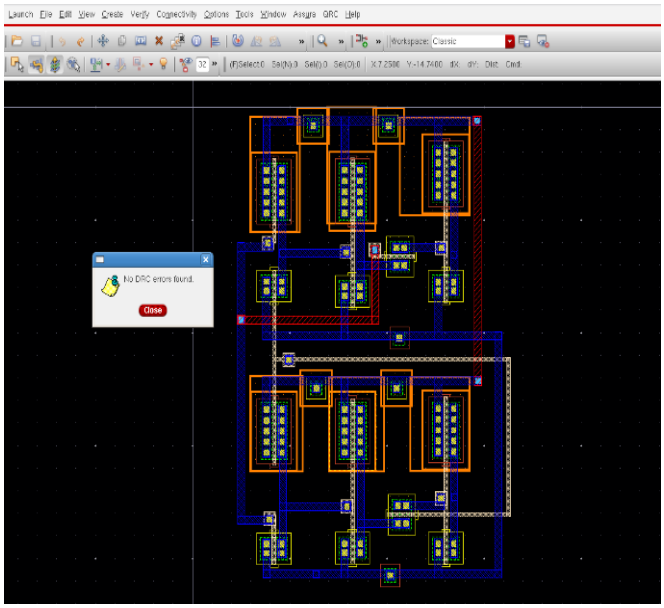

Fig. 14: Layout of Conventional PFD

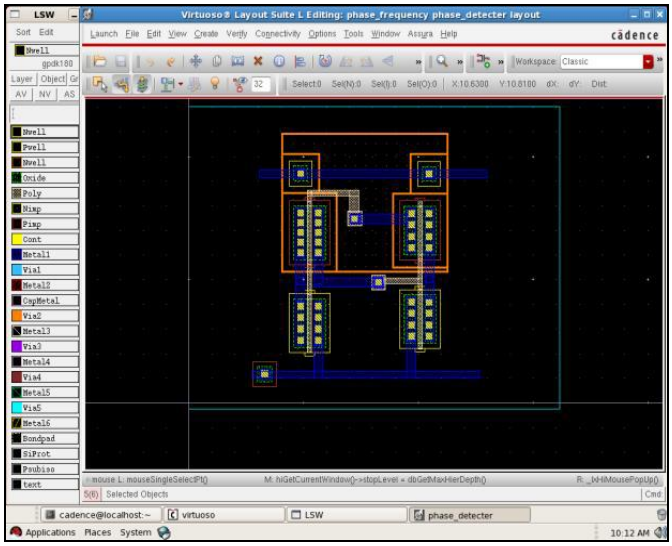

Fig. 15: Layout of PFD with GDI cells

Table 2 Performance comparison

Types of PFD	Power consumption	Maximum op. frequency	Dead zone
Conventional PFD	33.5uW	500MHz	100ps
PFD with GDI cell	8uW	5GHz	20ps

VI. Discussion and Conclusion

Comparison of maximum operation frequency between conventional PFD and PFD with GDI cell shows the variations of the maximum operation frequency with supply voltage. At 1.8V voltage supply the maximum operation frequency of the conventional PFD is 500 MHz whereas proposed PFD is.5 GHz .This indicates that proposed PFD is reliable in high speed applications

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