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HDL Design for Universal Novel Multi Clock Oscillator/Generator Soft Asic Ip Core for – Mega, Giga, Tera, Peta, Exa, Zetta, Yotta, Xona, Weka Clock Frequency Rate Eda Asic/Fpga Cards /Products

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***Abstract*—In Future Electronics, All the Products are 6th Sense based Hi-tech Smart Computing Electronic products and Applications, ASIC,SOC Card based Products and Applications will come to the market , Due to that , I Designed HDL Design for Universal Novel Multi Clock Oscillator / Generator Soft ASIC IP CORE FOR – MEGA, GIGA, TERA, PETA, EXA, ZETTA, YOTTA, XONA, WEKA CLOCK FREQUENCY RATE 6th Technology based All EDA ASIC Smart Computing Products and Applications. This Design Unit Basically Consists of 8:1 Multiplexer and Clock Generators/Oscillators of Giga, Tera, Peta, Exa, Zetta, Yotta, Xona, Weka bits / Second. All these Clock Frequencies are generated by using Simple Clock Divider Implemented through Simple Counter based on No of Clock Cycles Required for Each Complete Clock Cycle/Pulse. Suppose for Giga Hertz Speed, $2^{30}/2$ or $10^{9}/2$ Clock cycles required for active low and high clock pulse of 1 Giga Hertz Clock Cycle. Similarly for Tera Hertz Speed $2^{40}/2$ or $10^{12}/2$, Peta Hertz Speed $2^{50}/2$ or $10^{15}/2$, Exa Hertz $2^{60}/2$ or $10^{18}/2$, Zetta Hertz $2^{70}/2$ or $10^{21}/2$, Yotta Hertz $2^{80}/2$ or 10^{24},Xona Hertz $2^{90}/2$ or 10^{27} ,Weka Hertz $2^{100}/2$ or 10^{30} clock cycles require for all new innovative future generated. Advanced High Computing Electronic Products/Applications like wireless, telecom, automation, consumer, medical, graphics. Data Bus Communication and Networking, Avionics, Aerospace, Automotive, Cloud and Internet Supercomputing, Cluster and Super Grid Computing. Programming Done by using VHDL and Verilog HDL Languages. Software Design Implementation through Xilinx ISE 9.2 i IDE Hi-tech Engineering Software Design Tool/Altera Quartus II Development Tool. Testing and Design Reconfiguration / Debugging Implementation Done by FPGA SPARTAN III /Altera Stratix II Development Board.**

***Keywords*—EDA – Electronic Design Automation, HDL – Hardware Description Language, ASIC- Application for Specific Integrated Circuit, ISE- Integrated Software Environment, IDE – Integrated Development Environment.**

I.INTRODUCTION

Clock Oscillator/Generator is continuous/Discrete periodic pulse generator for generate specific possible number of Pulse Events in the form of pulses for performance of particular operation. It is the Heart of every Electronic Product / Applications Either Digital /Analog. Clock Oscillator design Derived from Digital Oscillators / Generators like Damped, Under Damped, over Damped Triggered Oscillator Models for generation of clock frequency oscillations. This is an important component for processing and controlling of signals in Electronic Design Automation based signals and system Software and Hardware Products and Applications. A common layman can understand that every Hi-tech Digital electronic design / product / application require Clock Oscillator for synchronizing, processing, controlling signals of systems. Simply it is the "Heart of Electronics". This clock oscillator / Generator generates different types of signals like unit step, Square, ramp, impulse, sawtooth, triangular wave based on the different transforming techniques. Now a Days in Modern and Future Electronics Design and Automation products and applications require clock oscillator / generator. Applications like wireless and telecom, Data Communication and Networking, Multimedia communication, Real-time Smart Computing Electronics like cloud, Internet, cluster, super grid computing, Industrial Design Automation Cellular and Mobile ,Hi-tech Consumer and Medical electronics, Graphics and Image ,video processing , Avionics/Aerospace, Automotive, Advanced Processor and Controller IP Cores , memory products/Cards etc. clock oscillator /wave form generator suit for Improvement of speed ,processing and controlling of all electronic system products from simple gate to complex SOC's / Cards/Interface Cards. In Future Electronic system products are 6th Sense Electronics based Hi-tech Smart Computing products due to that I designed Universal Clock Oscillator for generation of clock frequencies of Mega, Giga, Tera, Peta, Exa, Zetta, Yotta, Xone, Weka bits per second speed for all 6th sense based electronic system products and applications for Improvement of speed and performance.

I Designed and Developed RTL Design and Logic Architectures and HDL Soft IP Cores Development using VHDL and Verilog HDL for New Innovative Mega, Giga, Tera, Peta, Exa, Zetta, Yotta, Xona,

Wetta Hertz oscillators based on different clock cycles. This Design Unit Basically Consists of 8:1 Multiplexer and Clock Generators/Oscillators of Giga, Tera, Peta, Exa, Zetta, Yotta, Xona, Weka bits / Second. All these Clock Frequencies are generated by using Simple Clock Divider Implemented through Simple Counter based on No of Clock Cycles Required for Each Complete Clock Cycle/Pulse. Suppose for Giga Hertz Speed, $2^{30}/2$ or $10^{9}/2$ Clock cycles required for active low and high clock pulse of 1 Giga Hertz Clock Cycle. Similarly for Tera Hertz Speed $2^{40}/2$ or $10^{12}/2$, Peta Hertz Speed $2^{50}/2$ or $10^{15}/2$, Exa Hertz $2^{60}/2$ or $10^{18}/2$, Zetta Hertz $2^{70}/2$ or $10^{21}/2$, Yotta Hertz $2^{80}/2$ or 10^{24},Xona Hertz $2^{90}/2$ or 10^{27} ,Weka Hertz $2^{100}/2$ or 10^{30} clock cycles. This clock acts as a driver for every electronic system / product. Clock Oscillators mainly used for Randomizers for generation of Random frequencies for speed Improvement.

II. ARCHITECTURES

A) HDL Design ARCHITECTURES for Mega, Giga, Tera, Peta, Exa, Zetta, Yotta, Xona, Weka bits per second Clock Frequency Generators / Oscillators

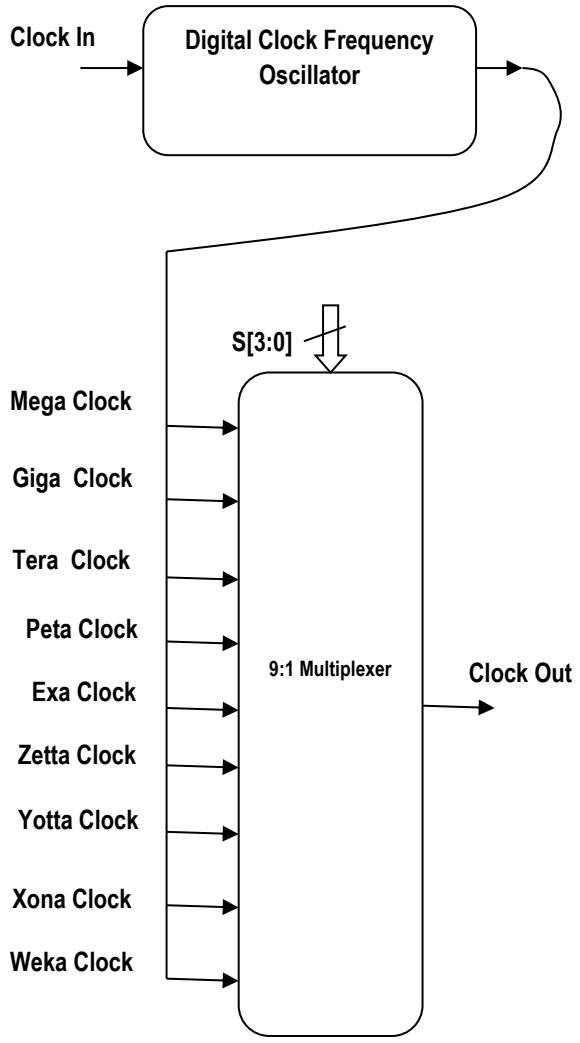

Figure 1. Novel Universal Multi Clock Oscillator/Generator

Description: This Design Unit Consists of 9:1 Multiplexer , Digital Clock Oscillator for generating and selection of different clock frequencies like Mega, Giga, Tera, Peta, Exa, Zetta, Yotta, Xona, Weka bits per second speed. These Clock Oscillators mainly used for new innovative-Future-Generated-mega,Giga,Tera,Peta,Exa,Zetta,Yotta, Xona, Weka Electronic Development FPGA,ASIC Boards/Cards. Based on the Number of Clock Cycles and generate different oscillator frequencies for Mega, Giga, Tera, Peta, Exa, Zetta, Yotta, Xona, and Weka Hertz Range.

B) DETAILED ARCHITECTURE s[3:0]

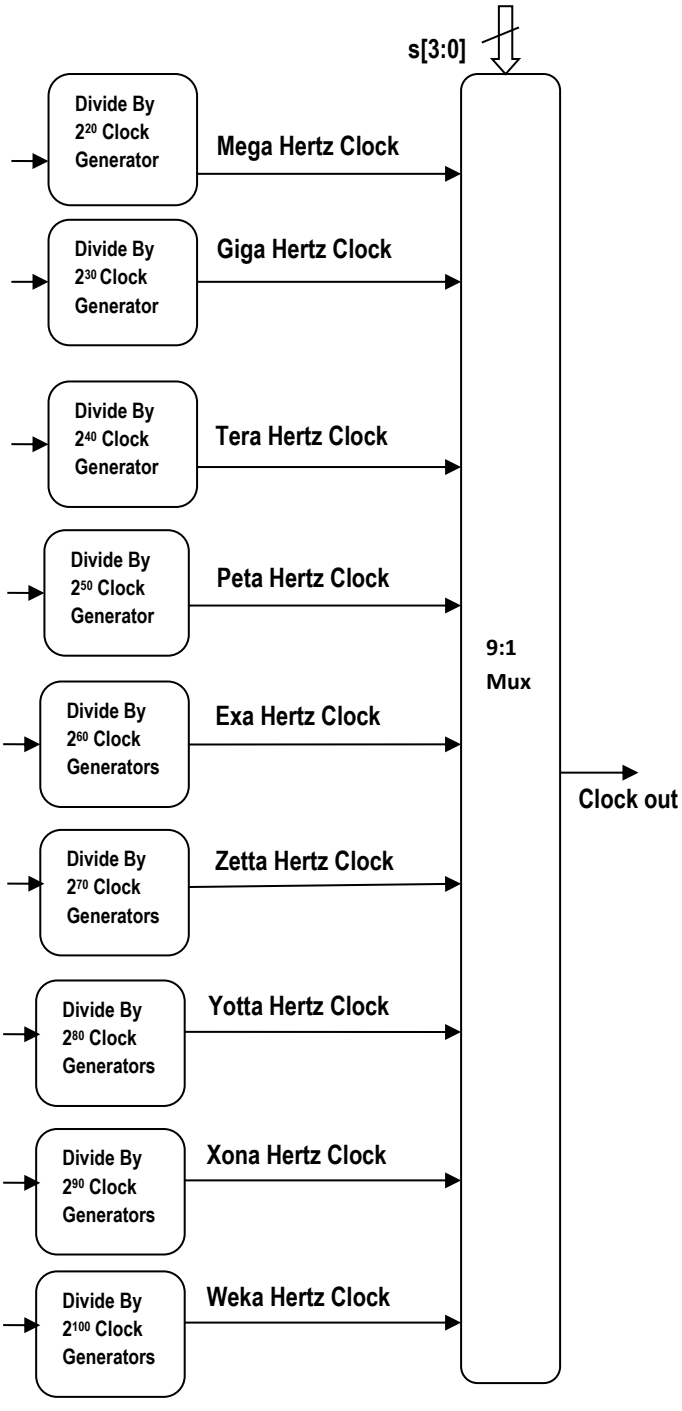

Figure 2. Novel Universal Multi Clock Generator Detailed Arc.

III.EDA-SOFTWARE–VLSI-ICDESIGN FLOW

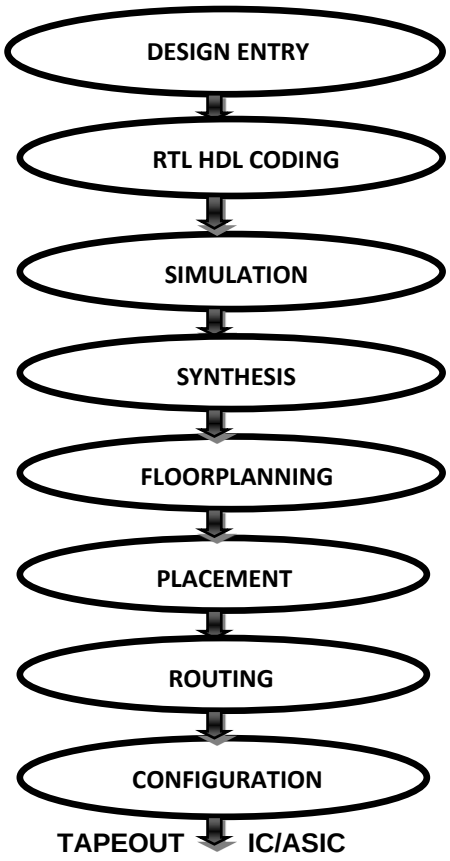

Figure 3. VLSI IC DESIGN FLOW

IV. FPGA DESIGN FLOW REPORTS

A) SIMULATION REPORT Universal Clock Generator

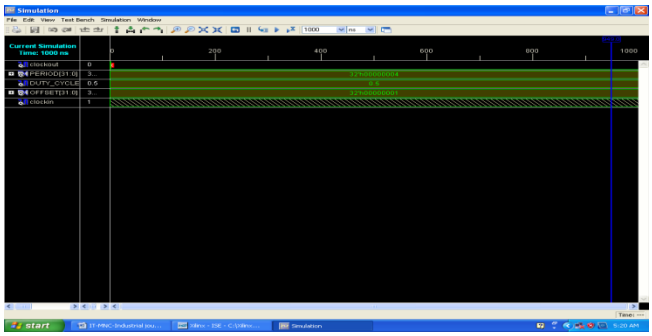

Figure 4. Simulation Report-Clock

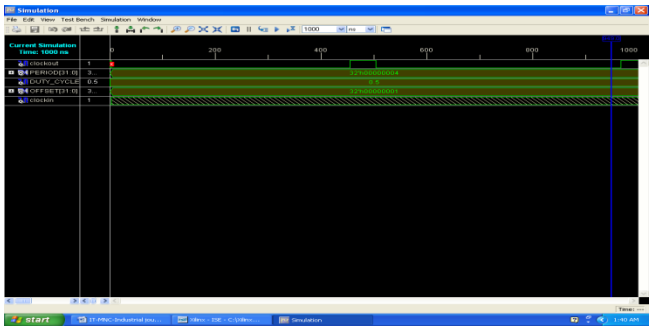

Figure 5. Simulation Report-Multi Clock

B) RTL DESIGN BLOCK-Multi Clock Oscillator

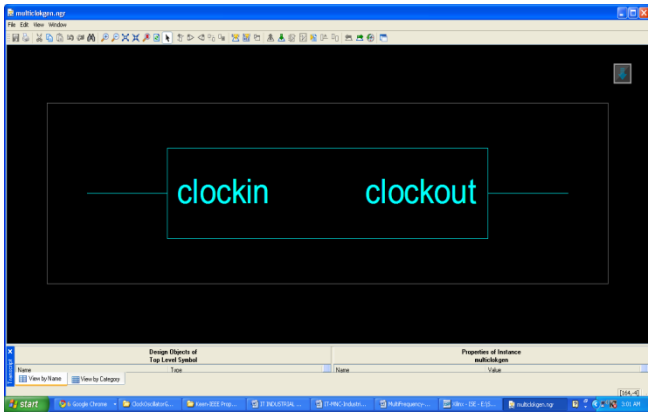

Figure 6. Multi Clock Oscillator RTL Design

C) RTL SCHEMATIC DESIGN BLOCK

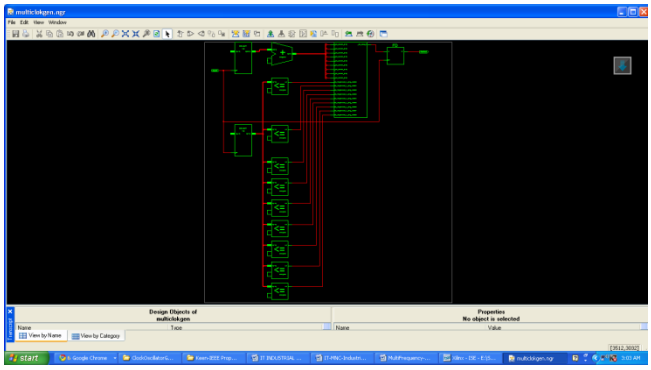

Figure 7. Multi Clock Oscillator Schematic

D) RTL SCHEMATIC INTERNAL LOGIC-Multi Clock

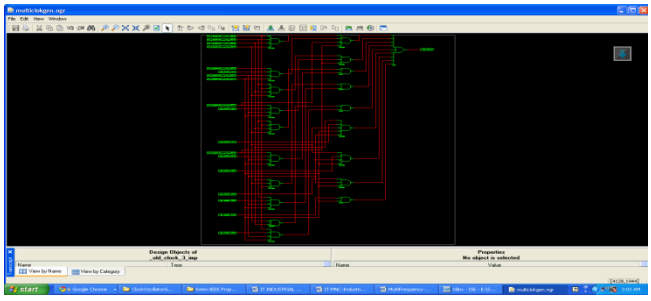

Figure 8. Multi Clock Schematic

E) FPGA PLACED DESIGN REPORT-Multi Clock

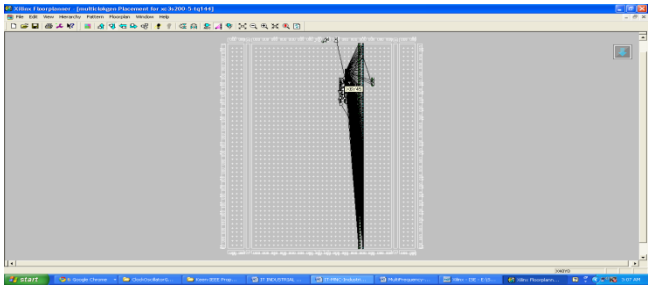

Figure 9. Multi Clock Oscillator Placed Design

F) FPGA ROUTED DESIGN REPORT

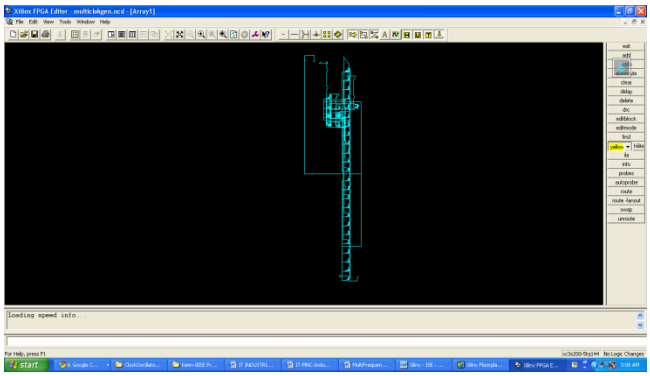

Figure 10. Multi Clock Routed Design Report

G) SYNTHESIS REPORT

```
=====================================
HDL Synthesis Report
Macro Statistics
# Adders/Sub tractors                 :1
 100-bit adder                       :1
# Counters                            :2
 100-C counter                       :1
 8-bit up counter                    :1
# Registers                           :1
 1-bit register                       :1
# Comparators                         :10
 8-bit comparator less equal         :10
=====================================
Final Register Report
Macro Statistics
# Registers                           : 109
 Flip-Flops                          : 109
=========================================
```

H) STA REPORT

```
Data Sheet report:
-----------------
All values displayed in nanoseconds (ns)
Clock clockin to Pad
------------+------------+-----------------+--------+
 | clk (edge) |          | Clock |
Destination | to PAD |Internal Clock(s) | Phase |
------------+------------+-----------------+--------+
clockout    |   8.481(R)|clockin_BUFGP    |   0.000|
------------+------------+-----------------+--------+
Clock to Setup on destination clock clockin
---------------+---------+---------+---------+---------+
 | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
Clockin        | 12.051  |         |         |
---------------+---------+---------+---------+---------+
```

V. CONCLUSION:

The AIM of Designed Universal Clock Oscillator is for 6th Sense Technology Based all latest and future Hi-tech Smart Computing Embedded & VLSI Products and Applications and also latest Tera,Peta,Exa,Zetta,Yotta,Xona,Weka Cards/Boards/SOC's. The Intention of Design is for provide Very High Speed and Performance and High Quality and Reliability Electronic Boards/Cards/SOC's, Products and Applications.

VI. FUTURE SCOPE:

Suit for Future Generated Smart Electronic Products and Applications, latest Advanced Hi-Speed Electronic Cards.

VII. REFERENCES

Bibliography

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Recently he delivered Invited lecture in University of Minnesota, Minneapolis USA.on Application of Kalman filtering for Power Electronics and Power systems. He has guided 5 PhD Students and currently guiding 8 PhD students.